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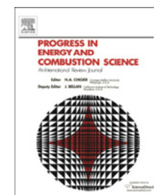

Heat and fluid flow in high-power LED packaging and applications

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ABSTRACT

Light-emitting diodes (LEDs) are widely used in our daily lives. Both light and heat are generated from LED chips and then transmitted or conducted through multiple packaging materials and interfaces. Part of the transmitted light converts into heat along the light propagation; in return, the accumulation of heat leads to the degradation of light output. The accumulated heat negatively influences the reliability and longevity of LEDs, and thus thermal management is critical for LED packaging and applications. On the other hand, in LED packaging processes, many fluid flow problems exist, such as phosphor coating, silicone injection, chip bonding, solder reflow, etc. Among them, phosphor coating is the most important process which is essential for LED performance. Phosphor gel is a kind of non-Newton fluid and its coating process is a typical fluid-flow problem. Overall, since LED packaging and applications present many heat and fluid flow problems, obtaining a full understanding of these problems enables advancements in the development of LED processes and designs. In this review, the emphasis is placed on heat generation in chips, heat flow in packages and application products, fluid flow in phosphor coating process, etc. This is a domain in which significant progress has been achieved in the last decade, and reporting on these advances will facilitate state-of-the-art LED packaging and application technologies.
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1. Introduction

Light-emitting diode (LED), as a type of solid-state lighting (SSL), is a lighting technology that arguably constitutes the greatest advancement in the lighting industry in the previous century [1–3]. In an LED, electricity is converted into light. It is well recognized that LEDs offer the following advantages. (1) Energy savings: LED requires less energy to emit equivalent light compared to other light sources. (2) Long lifetime: Due to their compact physical characteristics, LEDs are also more long-lasting than other lamps. Incandescent bulbs tend to last 1000 hours as heat destroys the filament, and fluorescent lamps tend to last 10,000 hours. While LEDs can last over 50,000 hours or more in theory. (3) Environment-friendly characteristics: Unlike fluorescent lamps, there is no mercury in LEDs, which is environment-friendly whenever the LEDs are discarded. (4) Wide color temperatures: LEDs provide a wider range of color temperature (4500 K–12,000 K) and a wider operation temperature (−20 °C to 85 °C). (5) Quick startup: LEDs do not have low-temperature startup problems, which is different from many other lighting sources, such as metal halogen lamps. Based on the above advantages, so far, LEDs have been considered as the fourth generation of light sources [1,4]. They have been extensively applied in our daily lives, including street lamps, backlighting, automobile headlamps, and general lighting. It is believed that LEDs will benefit the whole world even more extensively and profoundly in the future [5,6]. Due to LEDs' contribution to the whole of human society, the 2014 Nobel Prize in Physics was awarded to three scientists for the invention of efficient blue LEDs based on gallium nitride (GaN) [7].

1.1. Basic knowledge of LED

For high-power LED chips, the key part is the "PN junction" where a quantum well or multiple quantum well (MQW) layers are sandwiched with a p-GaN layer and an n-GaN layer [1]. In a PN junction, the "P" material contains an excess of positive charges (also called holes) due to the absence of electrons. The "N" material contains an excess of negative charges due to the presence of electrons. To understand the lighting principle, we can consider an unbiased PN junction. Fig. 1 shows the PN energy band diagram. The depletion region extends mainly into the p-side. There is a potential barrier from E_c on the n-side to the E_c on the p-side, which is called the built-in voltage, V_0. This potential barrier prevents the excess free electrons on the n-side from diffusing into the p-side. When a voltage V is applied to the junction, the built-in potential is reduced from

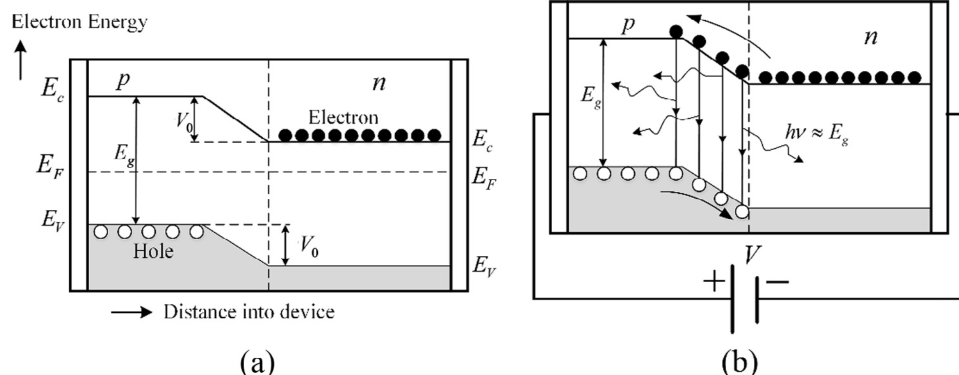


Fig. 1. LED lighitng principle. (a) The energy band diagram of a PN junction without any bias. Built-in potential V_0 prevents electrons from diffusing from the n-side to the p-side. (b) The applied bias reduces V_0 and thereby allows electrons to diffuse or be injected into the p-side, resulting in light emission when electrons and holes recombine.

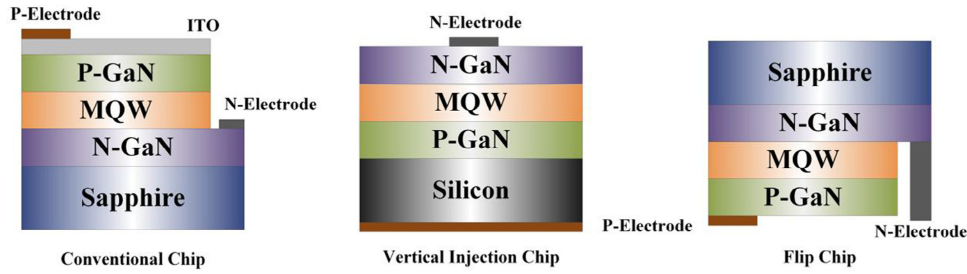


Fig. 2. Schematic diagram of three types of LED chip architectures.

V_0 to V_0–V. This allows electrons from the n-side to get injected into the p-side and recombine with the holes there, resulting in spontaneous emission of photons (light).

To make the PN junction applicable to LEDs, different types of LED chips have been proposed. Fig. 2 presents three kinds of LED chip designs, which include the conventional chip, the vertical chip, and the flip chip. The conventional chip generally utilizes sapphire as the substrate for epitaxial growth. p- and n-electrodes are arranged at the two edges of the top surface of the chip. However, the thermal conductivity of the sapphire substrate (~20–40 W/(m·K)) is low compared to that of silicon (~150 W/(m·K)); so, it establishes a barrier for the chip heat dissipation. To improve this shortcoming of conventional chips, vertical injection chip and flip chip designs have been proposed [8]. Unlike the conventional chip, the electrodes in the vertical injection chip are arranged at the top and bottom of the chip. Such an electrode structure can improve the uniformity of current density distribution, resulting in MQW utilization efficiency enhancement and lighting emitting efficiency (LEE) improvement. Compared to conventional LEDs, the flip-chip LED is “flipped-over” or inverted [9]. The electrodes are arranged at the bottom of the chip, and light is emitted from the top surface. As a result, such structure avoids light absorption by the metal contact in conventional chips, and the utilization efficiency of the MQW is enhanced. Moreover, in the flip chip, the sapphire is arranged as the top layer, which can, to a certain extent, solve the poor heat dissipation problem of conventional chips. Heat generated in the flip chip LED can be dissipated to the packaging board through the highly thermally conductive contact electrodes rather than sapphire. Thus, flip chips possess better thermal characteristics.

Blue LED chips cannot be directly used in application products, and it is necessary that they are packaged and emit white light. Currently, the most common packaging method of producing white light is shown in Fig. 3. Under the blue light emission, yellow phosphors (such as cerium-doped yttrium aluminum garnet, YAG:Ce^{3+}) could emit yellow light, and the mixture of transmitted blue and yellow lights generate white light. By controlling the energy ratio of blue light and yellow light, the white light can be obtained at different color temperatures. This method is easy and simple to handle with high luminous efficiency. Thus, it has been widely adopted in industry.

1.2. LED packaging process and its application

Fig. 4 shows the LED industry chain. It consists of three categories: the upstream, the midstream, and the downstream. Epitaxy growth is the first step in the upstream, in which the emitting layer, cladding layer, buffer layer, reflector, etc., are accomplished in this process. The metal organic chemical vapor deposition (MOCVD) is the main method to produce blue, green, and ultraviolet epitaxy materials, such as GaN or GaAs. Different colors of LEDs can be made by employing different types of epiwafer. After the fabrication of LED wafers in the MOCVD chamber, the chip manufacturers will dice the wafer into LED chips with positive and negative electrodes. The chip manufacturing process includes film plating, lithography, chemical or iron etching, scribing, etc. In Fig. 4, the midstream industry is referred to as packaging. Through the upstream, we can obtain blue light LED chips. Before the application, we should convert the blue light emitted from the blue light LED chips into white light LEDs by packaging. The typical way to convert blue light into white light is shown in Fig. 3. Currently, there are many types of LED packages. According to the number of LED chips, it can be categorized as single-chip package, multiple-chip package, or chip-on-board (COB) package. The downstream industry refers to the integration of LED modules into lighting luminaries and systems aimed at different applications, such as street lamps, backlighting units, general lighting, etc.

From the industry chain of high power LEDs, it is seen that packaging constitutes an essential step from LED chip to applications. Packaging not only can ensure better performance of LED devices by enhancing reliability and optical characteristics, but can also realize control and adjustment of the final optical performance. A typical lead-frame LED package and the function of each part are shown in Fig. 5. In this LED packaging, the LED chip is used to emit blue light, but it will generate heat as well. The solder is used to bond the chip onto the copper slug. The copper heat slug is used to dissipate the heat. The lead-frame and boding wire are utilized for electrical interconnection. The optical lens and phosphors are used to control the lighting performance and light conversion. The

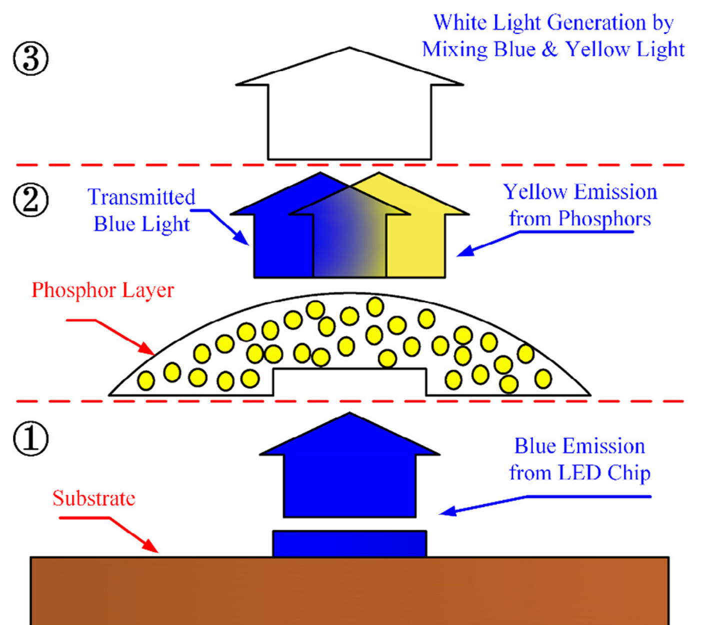


Fig. 3. Typical packaging method to produce white light based on blue LED chips.

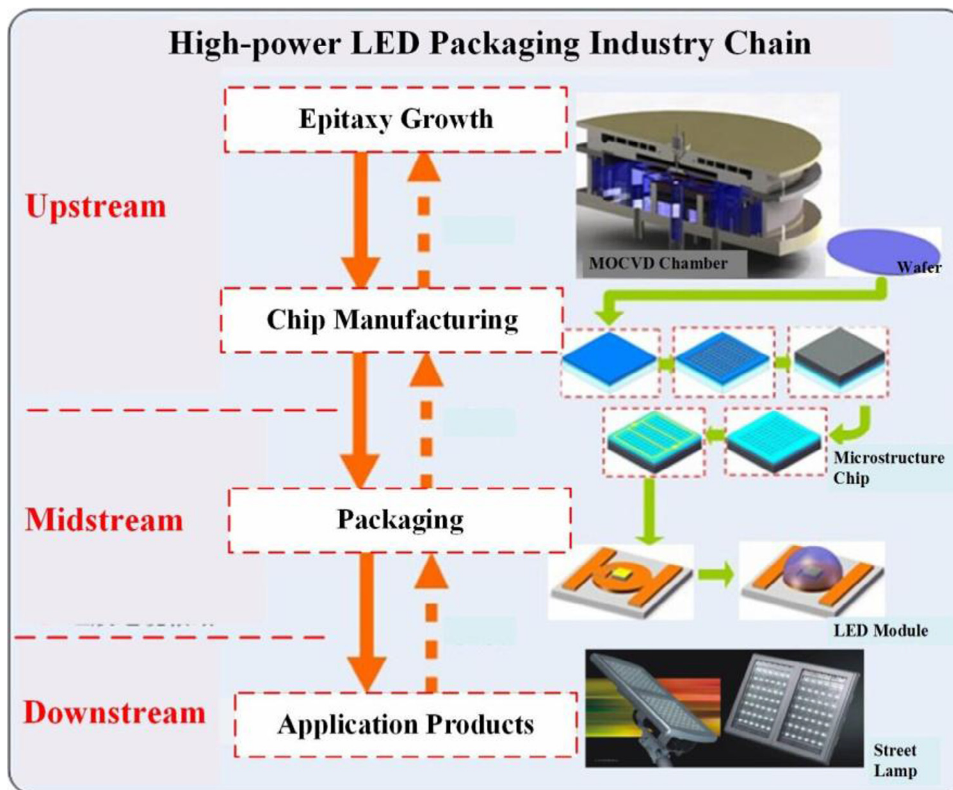


Fig. 4. LED industry chain.

moulding compound is employed to maintain the lead-frame and copper heat slug, and to fasten the optical lens.

To reach the above functions, the standard LED packaging process is formed in industry, and is shown in Table 1. Step by step, the packaging processes are as follows.

(a) Chip bonding: The chip is bonded onto the substrate by solder. The solder is a kind of non-Newton fluid cured in the reflow process. It is a complex problem coupled with fluid flowing, fluid curing, and heat dissipation. The solder will cure while flowing in the reflow process, and temperatures influence the flowing characteristics greatly.

(b) Wire bonding: The electrodes of the chip are connected to the lead frame by the bonding wires. The bonding wires can be gold, copper, aluminum, etc.

(c) Phosphor coating: Phosphor silicone matrix of a certain concentration is dispersed onto the chip surface to form a phosphor layer. The purpose of coating the phosphor layer onto the blue LED chip is to convert part of blue light into yellow light, resulting in white light after color mixing. Phosphor coating is a typical fluid flowing problem, and the final phosphor layer's morphology is dependent on the flowing characteristics, and determines the final optical performance of LEDs. In addition, phosphor particle sedimentation may occur in the silicone due to the larger density of phosphors, which plays a negative role in the final optical performance. Therefore, phosphor particle distribution also needs to be well-controlled during coating. Phosphor coating constitutes an important and difficult problem. Understanding the flowing and thermal properties can greatly help to

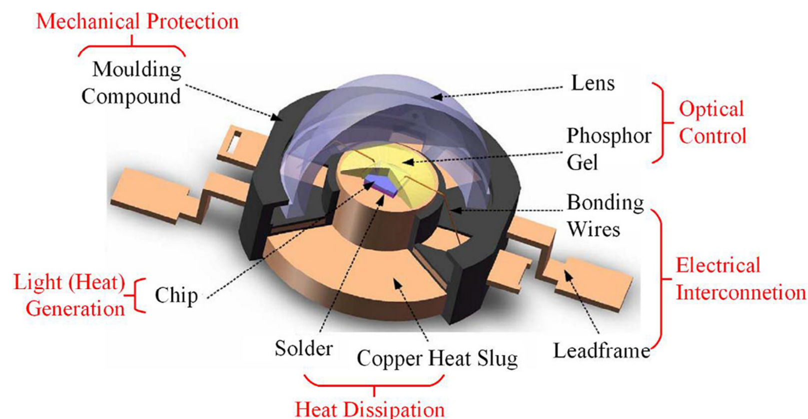


Fig. 5. Typical LED packaging structure and functions.

Table 1
Typical packaging processes and their applications for white LEDs.

Process Steps	Schematics	Descriptions
Chip bonding	Reflector; Chip; Solder; Substrate	• To attach the LED chips onto the substrate for fastening and heat dissipation • Coupled with thermal interface resistance control
Wire bonding	Bonding Wires	• To realize electrical interconnection
Phosphor coating	Phosphor Silicone Matrix	• To convert blue light into yellow emission • Coupled with phosphor coating fluid flow
Lens laying	Optical Lens	• To fasten the optical lens to the mechanical structure
Encapsulation	Silicone	• To fill the interspace with silicone and to protect the chip, bonding wires, etc. • Silicone flow
Module application in luminary	LED Chip; LED Module; Board; Heat Sink	• Thermal interface resistance, thermal spreading resistance, and thermal dissipation from component to ambient

control the flow and reveal potential new processes for phosphor coating.

(d) Lens laying: The lens is embedded into the molding compound by the mechanical structure. The lenses, as the dominant optics, are the key components to realize different optical requirements of applications. Conventional lenses are hemispherical, but their optical performances are poor. Freeform lenses possess better optical performance, and can be designed to suit various illumination requirements.

(e) Encapsulation: The silicone is filled into the interspace between the lens and the molding compound to protect the chip and bonding wires. This step is a total fluid flowing problem since the silicone curing at room temperature could be omitted. The injection pressure and nozzle size are the key parameters that should be well-controlled.

Through the above packaging steps, white LED modules can be obtained. However, the typical power for a single module is about 1 W, which is not bright enough for lighting. Therefore, we usually assembly many modules into LED lamps, whose power ranges from several watts (e.g., light bulbs) to hundreds or thousands of watts (e.g., street lamps, search lights, etc.). For such lighting fixtures, the heat generated in tiny chips will conduct to the ambient through multiple materials and interfaces. Thus, there are many thermal resistances that influence this heat transfer process, such as interfacial thermal resistance, thermal spreading resistance, and component-to-ambient thermal resistance.

1.3. Existing heat and fluid flow problems

Table 1 shows the LED packaging processes step by step. It can be seen that there are many heat and fluid flow problems in LED packaging and applications. Among them, three typical problems, i.e. heat generation, phosphor flow, and heat dissipation, as shown in Fig. 6, are mainly discussed in this review due to the space limitations. The three problems are introduced in detail as below.

Firstly, LED chips are considered to be the primary heat source in LED packages. The mechanism of heat generation in LED chips is the non-radiative recombination process, which is dependent on the materials of MQWs. The current power conversion efficiency for blue LED chips is about 55%, and thus 45% of the input electrical energy is directly converted to heat [10]. As previously stated and shown in Fig. 3, along the light propagation, part of the light converts into heat, and thus currently ~70% of the input electrical energy converts to heat in LED products.

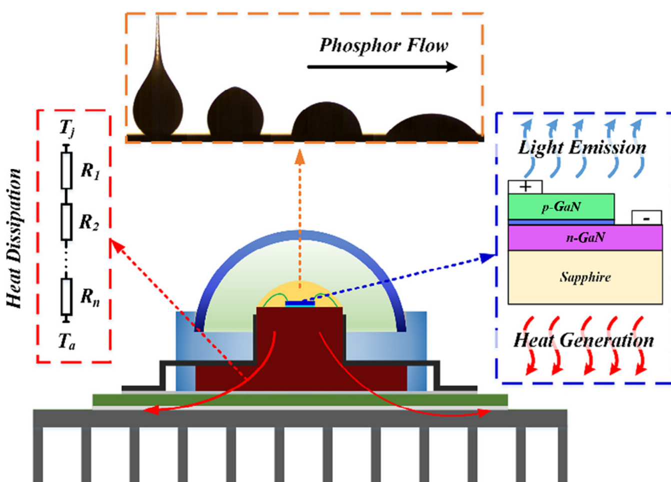


Fig. 6. Schematic of three typical problems in LED packaging, i.e. heat generation, phosphor flow, and heat dissipation.

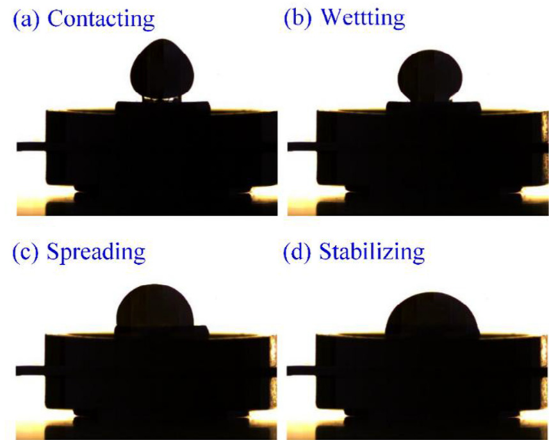


Fig. 7. Flowing process of phosphor gel on LED package.

Secondly, phosphor-embedded silicone matrix or phosphor gel, as can be seen from Fig. 3 and Table 1, is the key component that converts part of the blue light into yellow light, so as to finally generate white light. The phosphor gel is a kind of non-Newton fluid, which may cure after a period of time, and the curing time can be shortened when heated [11–13]. Fig. 7 shows the phosphor gel flowing process, which includes four steps: contacting, wetting, spreading, and stabilizing. It can be seen that after dispensing a drop of phosphor gel onto the LED chip, the phosphor gel contacts the chip first, then wets to cover the chip, then spreads along the heat slug, and finally stabilizes to form a convex shape. Meanwhile, in the flow process, the phosphor particles may settle due to the gravity effect, which would cause non-uniform particle distribution in the gel. It has been demonstrated that phosphor gel morphology and particle distribution play important roles in determining the final optical characteristics of white LED packages [14–18]. Improper phosphor gel morphology and particle distribution may cause poor color characteristics, i.e., blue rings or yellow rings, at the edge of the lighting pattern, as shown in Fig. 8. The flowing property of the phosphor gel should be well considered in the phosphor coating process in LED packaging. In addition, not only the heat generated in LED chips will be conducted to phosphors, but also the phosphors will generate heat during the photoluminescent process. The curing process of the matrix and silicone will occur simultaneously with the flowing process. High temperature will accelerate the curing process since silicone's viscosity increases greatly at high temperature. Therefore, the heat and fluid flow problems should be considered simultaneously in the phosphor coating process.

Thirdly, to prolong the reliability and lifetime of LEDs, we need to attempt to dissipate the heat generated inside of the package to

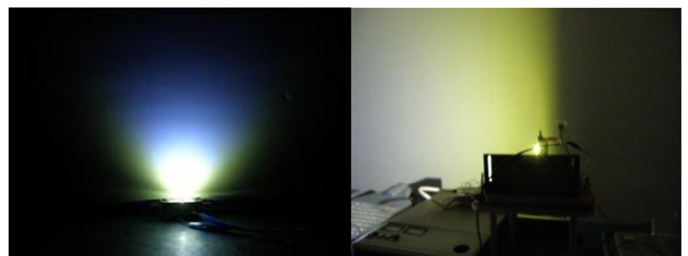


Fig. 8. Poor color characteristics in white LED packages due to improper phosphor coating.

the ambient and decrease the working temperature as much as possible because high temperature greatly deteriorates LEDs' performance. This is a systematic problem since it refers to heat generation, heat conduction and spreading, interface heat flow, and convection to the ambient.

It should be noted that the heat dissipation and fluid flow are usually coupled with each other and should be considered simultaneously.

1.4. Review arrangement

In this review, we began with an introduction of heat generation in LED chips, followed by a detailed review of phosphor coating process. Different phosphor coating processes were compared with a presentation of corresponding advantages and disadvantages. We then focused on the thermal management of LEDs, from chip to package, and from package to application. Thermal resistance constituted the parameter to evaluate the heat dissipation ability, and thus interfacial resistance, spreading resistance, and component-to-ambient resistance were introduced systematically. Finally, state-of-the-art thermal management solutions for LEDs were presented.

2. Heat generation of LED chips

LED chips are the core and functional part that produce light. Accompanying light emitting, heat will be generated within LED chips due to different kinds of nonradiative recombinations and other causes of photon annihilation. In this section, emphasis will be placed on analyzing the nonradiative recombination in the active region of LED chips and the factors that prohibit photon emission and lead to heat generation. Efficient LED chip designs from the perspective of epitaxial growth are reviewed with the purpose of suppressing the nonradiative recombination. In the active region of LED chips, Shockley–Read–Hall (SRH) recombination and Auger recombination are explained, whereas current crowding and electron overflow outside of the active region are also included in this section. Widely reported techniques to improve the light extraction efficiency of LED chips, such as roughing, photonic crystal integration, surface plasmonics, etc., will be covered. In the last part of this section, new LED chip designs are listed based on nanowire epitaxial growth techniques, which show great potential advantages over existing planar multiple quantum well (MQW) designs.

2.1. Heat generation due to nonradiative recombination

Fig. 9 shows the schematic of the band gap of semiconductor material, which has an electronic band structure determined by the crystal properties of the material. The discrete energy distribution is affected by the absolute temperature. Above absolute zero temperature, the existing energy levels are filled with electrons according to the Boltzmann distribution. The free electrons range from their bounds to a freely moving state which is called a conduction band (CB). The valance band (VB) is the highest range of electron energies in which electrons are bounded. The difference between CB and VB is called band gap or forbidden band, since ideally there is no electron energy state within this region [19].

The freely moving electrons in the meta-stable state exist in the CB until they fall to the VB and recombine with an electron hole. This process is referred to as recombination. There are two types of recombination within the active region of LED chips, i.e., radiative recombination and nonradiative recombination. For radiative recombination, the electron fills a hole in the valance band by releasing a photon with energy equal to the band gap energy of the semiconductor material [20]. This process is the foundation of the LED working mechanism. For nonradiative recombination, the releasing energy exists in the form of atom vibrations within the crystal, such as phonons; if the energy is not collected, it dissipates as heat. Apparently, the nonradiative recombination should be minimized for high device performance and low heat generation [21]. In the active layer of LED chips, there are two major nonradiative recombination processes, i.e., defect-related SRH recombination and Auger recombination, which will be described in detail below.

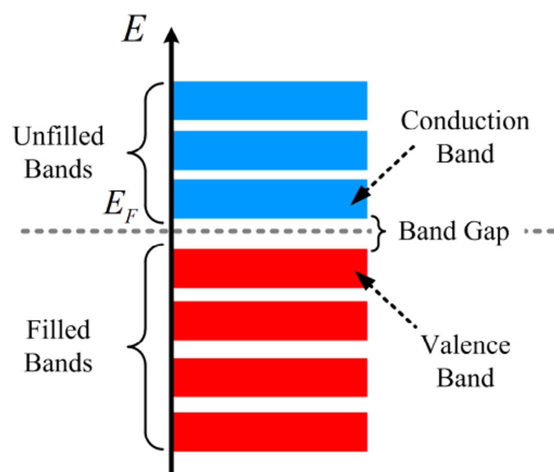


Fig. 9. Schematic of the band gap of a semiconductor material.

2.1.1. Shockley–Read–Hall (SRH) recombination

Fig. 10 shows the band diagram which illustrates the recombination process. In Fig. 10, the SRH recombination is used to describe the recombination of the electron and hole at the undesired energy level, which is created within the band gap by defects in the lattice. They were first investigated by Shockley, Read, and Hall in 1952 and were used as a model to study the nonradiative recombination caused by defects [22].

Defects in the crystal structure are the main cause of SRH nonradiative recombination. These defects include unwanted foreign atoms, crystallographic defects, etc. All of the defects have energy level bands that are different from the major semiconductor atoms. Therefore, the one or more new energy levels can be generated within the forbidden band gap. Unfortunately, these energy levels within the gap of the semiconductor are efficient recombination centers, especially when the deep level is near the middle of the gap. Detailed analytical expressions are obtained for the lifetime estimation of the SRH recombination [21]. These expressions reveal that when the trap level is at or close to the mid-gap energy, the lifetime is twice the minority lifetime, and the probability of SRH recombination is increased. Moreover, the increase of temperature will raise the nonradiative recombination probability. For simplicity, the recombination rate can be estimated by $R_{SRH} = An$, where A is the SRH recombination coefficient and n is the carrier concentration [23].

2.1.2. Auger recombination

Auger recombination describes the process in which the electron in CB gives off excess energy and recombines with a hole in VB. During this process, the excess energy is obtained by a second electron or hole instead of emitting the energy as a photon. The newly excited electrons or holes release their energy through collision with the crystal lattice and return back to the band edges.

The probability of Auger recombination increases with the concentration of charge carriers since this process is based on the ability of the charge carriers to exchange energy. The rate of Auger recombination can be expressed as $R_{Auger} = Cn^3$, where C is Auger

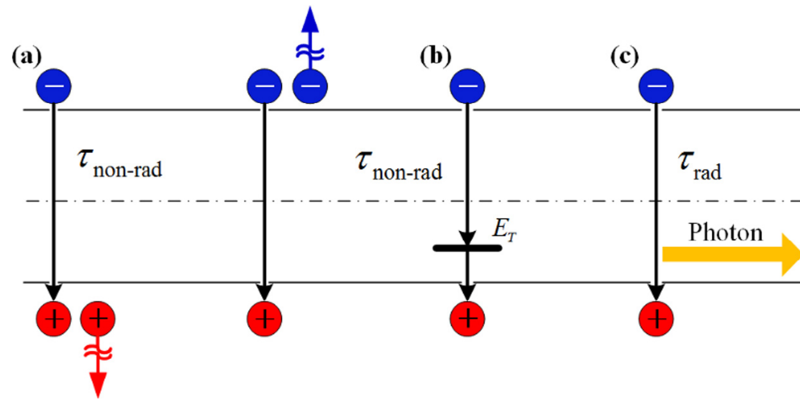


Fig. 10. Band diagram illustrating: (a) SRH recombination; (b) Auger recombination; and (c) radiative recombination (courtesy of Prof. E. Fred. Schubert from Rensselaer Polytechnic Institute, US).

recombination coefficient and n represents the carrier concentration. The coefficient C on the scale of 10^{-28}–10^{-29} cm^6/s for III–V semiconductors plays an important role [24]. Normally, C decreases with the increased energy band gap. According to the reported Auger recombination coefficients in Table 2, the simulation work adopts 10^{-30} cm^6/s for GaN-based LED chip design, which exhibits good prediction of device performance [29]. More detailed discussions about the Auger recombination coefficients can be found in a report by Cho et al. [30] At low carrier concentrations, the Auger recombination is neglected for practical reasons. However, at very high excitation intensity or the carrier injection current situation, n is much higher and Auger recombination should be considered.

2.1.3. Surface recombination

Nonradiative recombination also occurs at the semiconductor surface. At surfaces, the periodicity of the crystal lattice ends. Therefore, the band diagram will change at the surface since the strict periodicity of the crystal arrangement is perturbed. Additional electronic states will appear within the forbidden gap of the material [31]. Fortunately, surface recombination can be greatly reduced if the injected carriers are away from the surface. This can be realized by carrier injection under one contact which is smaller than the LED chip.

Table 2
Auger recombination coefficients reported for GaN-based LED chips.

Material	Auger recombination coefficient (cm^6/s)	Reference
$In_{0.10}Ga_{0.90}N$/GaN	1.5×10^{-30}	[25]
InGaN/GaN	3.5×10^{-31}	[26]
$In_xGa_{1-x}N$(x ~ 9%–15%)	1.4 to 2.0×10^{-30}	[27]
GaInN/GaN	2.5×10^{-31}	[28]

2.2. Heat generation due to current crowding and overflow

In Section 2.1, heat generation within the active region of LED chips due to the nonradiative recombination was introduced. Here, the focus will be placed on heat generated outside of the LED active region. Particularly, heat generation due to current crowding and overflow will be considered. The solutions are largely attributed to efficient LED chip design at the epitaxial and device level.

2.2.1. Current crowding in LED chips

In the realm of semiconductor physics, current crowding is used to describe a nonhomogeneous distribution of current density through the semiconductor at the vicinity of the contacts and over the PN junctions. As shown in Fig. 11(a), in conventional LED chips, the GaN layer grows on insulating substrates (e.g., sapphire) where electrons laterally spread from n-pad to p-pad. Due to this geometry, the finite resistance of the Ohmic contact and the confinement layer causes the current to "crowd" near the edge of the contact. As shown in Fig. 11(b), the current density distribution can be undesirably non-uniform. The current density could drop from 99 A/cm^2 at n-pad to 11 A/cm^2 at p-pad [32].

Due to the non-linear distribution of the current density, the crowding phenomenon becomes more severe in high power LEDs operating at large current density. The remarkable current concentration at the edges of p-type and n-type electrodes has a detrimental effect on device performance. On the one hand, the local increase

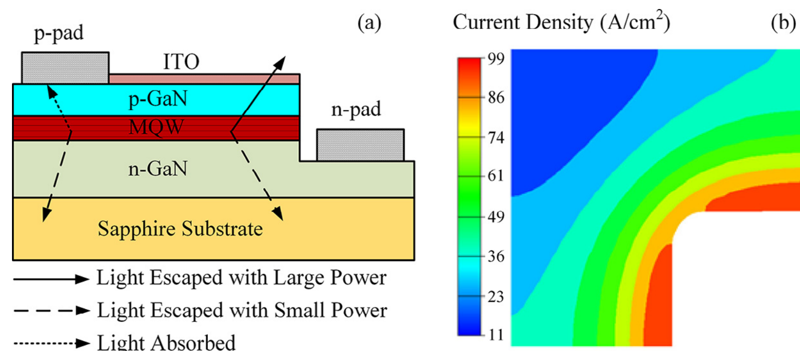


Fig. 11. Current crowding in GaN/InGaN LEDs on insulating substrates.

of carrier density leads to a high recombination rate, causing non-uniformity of light emission in the active region. This will induce localized overheating of the heterostructure at certain points and the formation of hot spots, whereas a large portion of the device remains inactive during operation. On the other hand, the inhomogeneous distribution of current will increase the electromigration effect, and voids are formed. Overall, current crowding will induce the local overheating of the heterostructure, lower the device performance, and increase the series resistance.

Various solutions have been proposed to reduce the current crowding problem, such as multi-fingered chip design [33]. Through simulations, Joshi et al. report that the current crowding problem is finally eliminated by a combination of multi-finger with delta-doping design. Vertical chip configuration can also solve this problem.

2.2.2. Current overflow in LED chips

Current overflow, also referred to as electron leakage, describes the process in which the energetic electrons move from n-type through the active region and recombine with holes in the p-type GaN without being confined in the active region. Since only the carriers confined in the active region are able to participate in the radiative recombination, the recombination caused by electron overflow generates unwanted heat. The current overflow is mainly caused by the higher carrier mobility of the electrons [34] (about 200 $cm^2 V^{-1} s^{-1}$) than that of the holes (about 10 $cm^2 V^{-1} s^{-1}$) [35]. The longer current spreading length caused by the higher mobility leads to fewer holes than electrons being injected into the active region. This is the reason why the AlGaN electron blocking layer (EBL) is usually adopted on the p-side of the active region.

Several theories have been offered to elucidate the reasons for, and eliminate, the effect of current overflow. The three most well-known are reviewed below. The first explanation concerns the poor hole-injection efficiency. Due to the large effective hole mass, low hole mobility limits the transportation length. In addition, with the purpose of effectively confining electrons, the Al content is raised. However, the high mole fraction of Al also prohibits hole injection [36–38]. Another explanation is that an ineffective EBL should be the cause of the electrons not being blocked. As we pursue high efficiency, large carrier concentration is injected into the LED chip. The increase of concentration and mobility makes it easier for electron transport. Even though a wide band gap design combined with an optimal 15% Al mole fraction in the EBL is adopted, this may not be sufficient for blocking the electrons. A further increase of Al fraction, in addition to the above mentioned reason, will also cause a polarization mismatch between AlGaN and GaN for the most widely researched and industrially accepted LED chip design grown in the c-direction [39,40]. One alternative explanation is that the active region in the form of MQW and EBL design are not able to fully confine the electrons. Those escaped electrons will enter the p-type region, non-radioactively recombine with holes, and generate heat. The probability of capturing electrons as a function of QW width was studied [41]. It was proven that increasing the QW thickness will raise the carrier dwell time, and therefore reduce current overflow [42]. Reports on modification of MQW and EBL have also been presented [43–47]. Moreover, there are some successful reports that explored LED growth on m-, a-, and other non-polar planes [48–50], which show lower polarization mismatch than c-plane LEDs.

2.3. Heat generation due to light confinement

Photons generated by radiative recombination may not be able to escape from the LED chip if they are totally internally reflected at the semiconductor–air interface. If the incident angle of the light ray is close to normal, they are effectively extracted outside of the LED chip; otherwise, they will be trapped inside [21] and converted into heat. This occurs because of the large refractive index difference of GaN (n = 2.5)/air (n = 1) interface. Total internal reflection (TIR) occurs when the incident angle exceeds the critical value $\theta_c = \text{asin}(n_1/n_2)$, which can be calculated based on Snell's law. The TIR leads to a narrow escape cone of only 23.5°, with an escape probability of only 4% from the top surface of the LED [51].

Techniques have been developed to improve light extraction efficiency (LEE), including photonic crystal, periodic surface texturing, surface roughing, patterned sapphire substrate, and reflectors using Al or Au electrodes. In this section, we will review the LEE improvement techniques separately at different locations of the LED chip.

Thin-film flip-chip (TFFC) design is widely used in current commercial LEDs, which possess high LEE as compared to that of conventional LED package design. Thin film LEDs could be realized by removing the sapphire substrate by the laser lift-off technique. On the other hand, flip-chip LEDs are achieved by submounting the p-GaN on a high reflectance-metallic mirror to form the vertical LED configuration. This allows photons to emit from the thicker n-GaN layer side, and enables a more flexible surface texturing and patterning process on n-GaN to enhance LEE without the potential effect on the InGaN QWs active region. The TFFC LEDs combine these two techniques, and therefore show great potential to enhance LEE.

2.3.1. Light emitting surface texturing and roughening

With the purpose of randomizing the light reflected at the semiconductor/air or GaN/substrate, surface texturing and roughening are widely-used methods. On the one hand, the straight propagation paths are disturbed, which enable multiple incidents on the interface to escape outside of the LED chip [52–54]. On the other hand, the spherical micro lens array can form a dome-shape at the interface to lead to more efficient LEE. Successful designs have been reported by researchers to improve LED output efficiency [51,53,55]. In addition, the direction of the emission light is unconfined, resulting in a Lambertian radiation pattern.

To increase the photon escape cone, a SiO_2/polystyrene micro lens array was deposited on the emission surface of the LEDs to form closed-packed lens arrays, as shown in Fig. 12 [51]. By adding the refractive index gradient, these arrays allow photons emanating from the QW to be scattered out of the LED structure with a larger photon escape cone from 23.5° to 39.8°. Using the SiO_2/PS micro lens arrays, the LEE of the LEDs can be increased with a larger photon escape cone, and Fresnel reflection loss can be reduced.

An efficient and cost-effective way to study surface texture in terms of LEE is through simulation. Zhao et al. studied the LEE of the four TFFC LEDs with different surface texturing by the three-dimensional finite difference time domain (3D-FDTD) method [53]. Fig. 13 shows the four simulation cases, i.e., flat top surface and top surfaces with SiO_2, SiO_2/polystyrene, and GaN micro lens array. They concluded that by adopting an optimal GaN micro lens diameter of 1 µm and p-GaN thickness of 195 nm, the LEE could be improved by 2.6 times.

Tsai et al. etched the light emitting layer of a vertical LED chip, and the corresponding textured structure is shown in Fig. 14(e). The etching process is shown in Fig. 14(a)–(d). As expected, the results shown in Fig. 14(f) indicate that the light output power of the top surface textured LEDs is much higher than conventional LEDs, which demonstrates that the top surface textures can improve LEE [55].

2.3.2. Photonic crystal to direct the light emitting shape

Photonic crystal is added on the top layer of conventional chip p-GaN. The dielectric constant of the crystal distributes periodically with special microstructures. Electromagnetic waves propagating inside will be modulated to form a photonic band gap. Then, the photon propagation is prohibited if its frequency falls within the range of the forbidden band. One solution is to use photonic crystals to gather the non-directional light emitted from

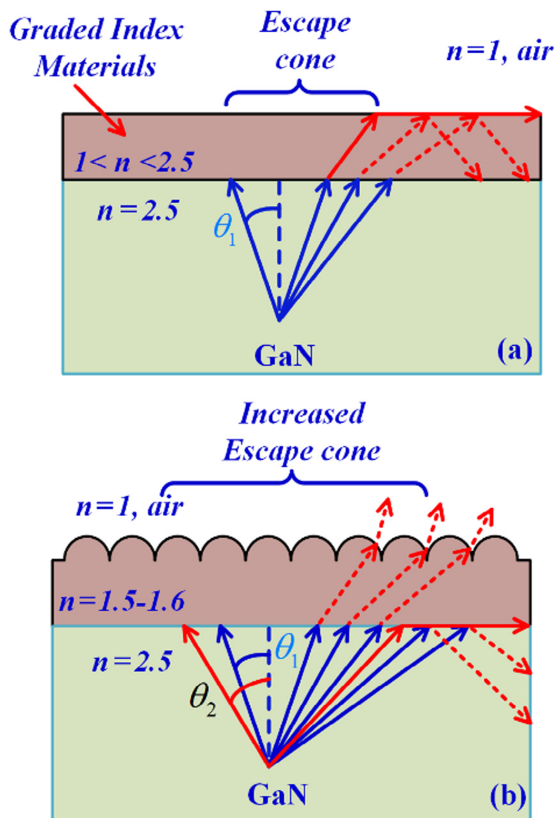


Fig. 12. (a) Schematic of LEDs coated with a planar layer of intermediate refractive index material between the semiconductor/air interfaces; (b) schematic of LEDs coated with the SiO_2/PS micro lens array, with a great increase in the photon escape cone (reprinted from Ref. 51 with permission of IEEE).

the active layer to contact the semiconductor; another solution is to use the air interface in an angle less than the critical angle of total reflection to avoid the absorption in the active layer. As shown in Fig. 15, Lai et al. [56] applied a two-dimensional (2D) photonic quasi-crystal (PQC) structure to the p-GaN surface of an LED by nano-imprint lithography and roughened the side of the n-GaN surface. The result shows that the efficiency of the LED with PQC is substantially improved compared to the conventional LED.

2.3.3. Patterned sapphire substrate (PSS)

When light emits from the active layer, a very large part will propagate backward directly to the sapphire substrate. Thus, to increase the escaping opportunity from the LED chip, patterned sapphire substrate offers a promising solution since it can break the TIR and increase the LEE [57]. Zhang et al. [58] fabricated three types of nanopatterned sapphire substrates (NPSS) by keeping the same heights at 200 nm and varying the pattern spacing from 0 nm to 120 nm. The scanning electron microscope (SEM) images of these structures are shown in Fig. 16(a)–(f). Here, FSS means flat sapphire substrate. The performance of the three types of patterned substrate LEDs was measured and compared to flat sapphire substrate LED. As shown in Fig. 16, it is clear that LEDs with a patterned substrate exhibit a large enhancement, and that the denser the patterns are packaged, the higher is the LEE of the LED.

2.3.4. Adding a reflector in flip chip LEDs

Metal reflectors can also be used to enhance LEE, and the distance between the active region and the metal reflector has a vital influence on the amplification of LEE. When the Ohmic contact layer is changed to metal, such as Ag or Au, most of the backward light will be reflected. However, although a large portion of light will be reflected, a part of the light is still absorbed by the metal or escapes

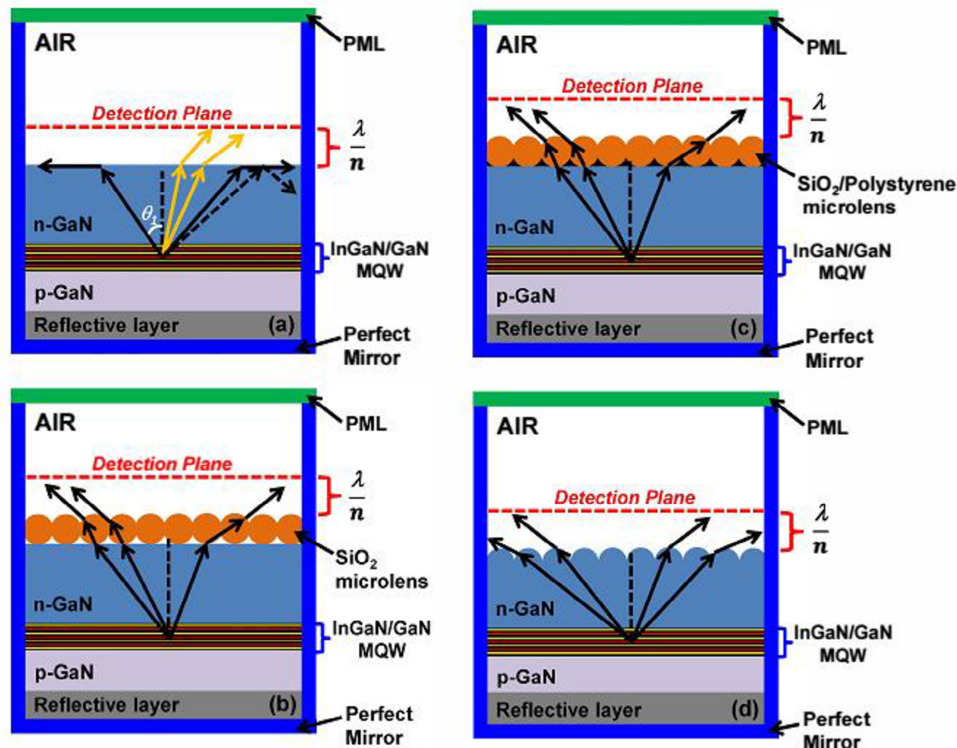


Fig. 13. Two-dimensional schematics of the TFFC InGaN QWs LED with: (a) flat surface; (b) SiO_2 micro lens array; (c) SiO_2/polystyrene micro lens array; and (d) GaN micro-hemispheres on top of the LED (reprinted from Ref. 53 with permission of IEEE). PML is short for perfectly matched layer.

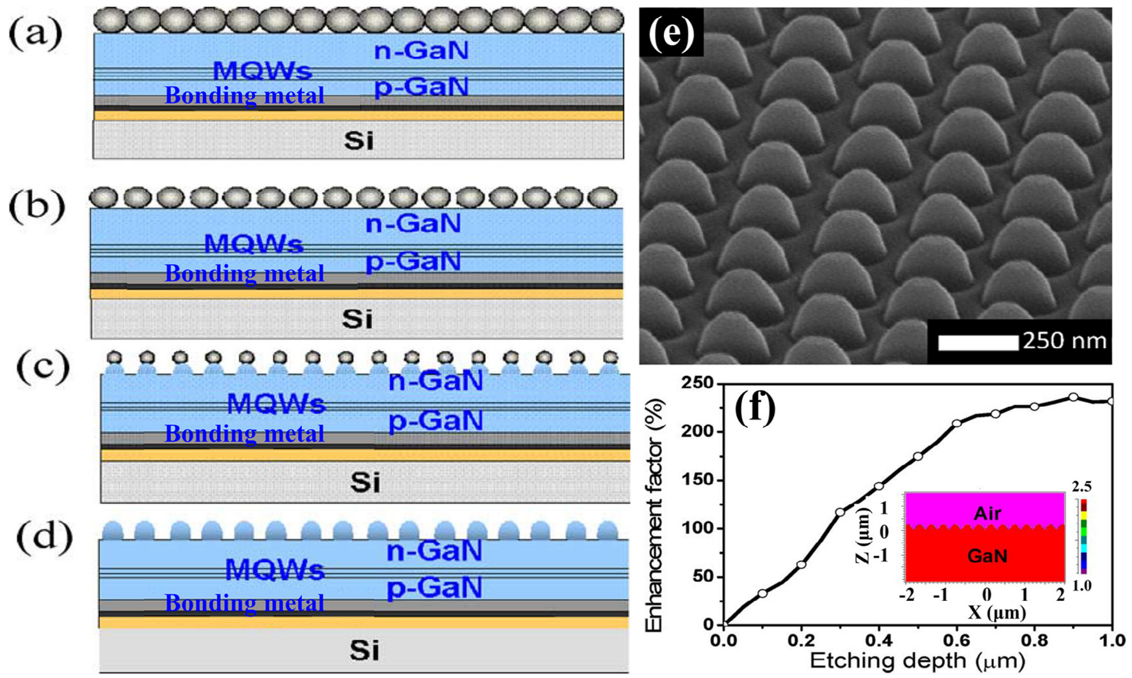


Fig. 14. (a–d) Schematics of the fabrication of biomimetic structures utilizing the PS nanospheres on the n-type GaN layer. (e) SEM image of the fabricated biomimetic surface structures. (f) Enhancement of light output power versus the height of biomimetic surface structures. The inset shows the simulated index profile (reprinted from Ref. 55 with permission of IEEE).

through the layer. The escaped amount of light will increase if the top surface of the metal is rough. Therefore, researchers focus on novel structures at the top surface of the metal layer to return the back light. Jan et al. [59] put forward a new structure at the interface between the metal layer and the semiconductor. Specifically, they added an n-shaping layer, as shown in Fig. 17(a), which can enhance the total reflectance of these layers at the bottom of the device. As a result, the LEE increased up to 50% compared to the previously reported values. The specific total output light flux is shown in Fig. 17(b).

2.4. Future trends of LED chip design with low heat generation

Based on the above analysis and an understanding of heat generation within LED chips, efforts have been made to increase the probability of radiative recombination, and thus reduce heat generation within the active region. From an epitaxial perspective, LED chips evolve from p–n junction to double heterojunction and MQW design. The carriers are well confined within the active region, and the recombination probability is greatly improved. Better epitaxy design, such as an optimal electron blocking layer, will soften the current overflow issues. At the chip level, the sapphire substrates with high thermal resistance in conventional LED chip design are replaced by the vertical or flip chip design. This trend not only improves thermal conductivity, but also overcomes the current crowding problem. Moreover, a large portion of light will be extracted from the LED chip to reduce the photon annihilation which generates heat. On the light emitting surface of LEDs, surface texturing and roughening, as well as photonic crystals, are adopted to improve light output efficiency. Patterned sapphire substrate and reflector at the metal contact are also proven to constitute effective candidates to increase LEE.

In the future, it can be reasonably assumed that researchers and industry will continue to pursue high efficiency, brightness, and low cost GaN-based solid state lighting technology. In addition to adopting the above methods to reduce heat generation, obtaining usage

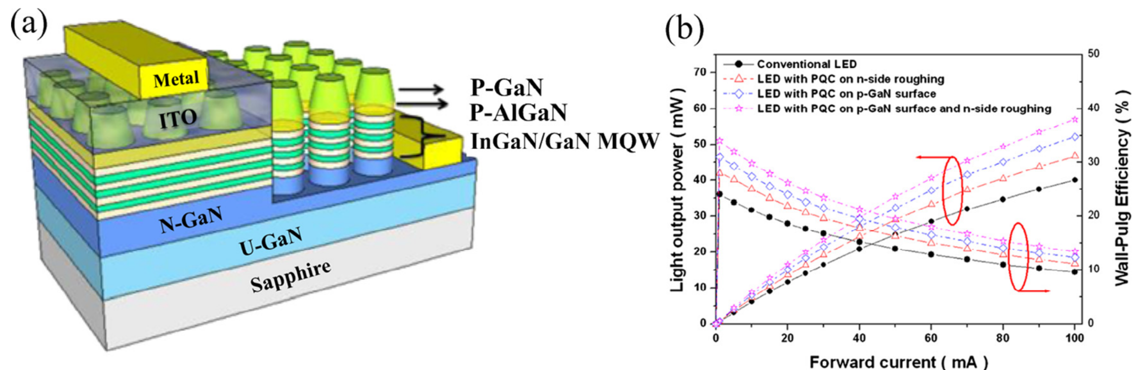


Fig. 15. (a) Schematic diagram of GaN-based LEDs with the PQC structure on the p-GaN surface and n-side; (b) light output power–current and wall-plug efficiency characteristics of LED with/without PQC structure (reprinted from Ref. 56 with permission of Springer).

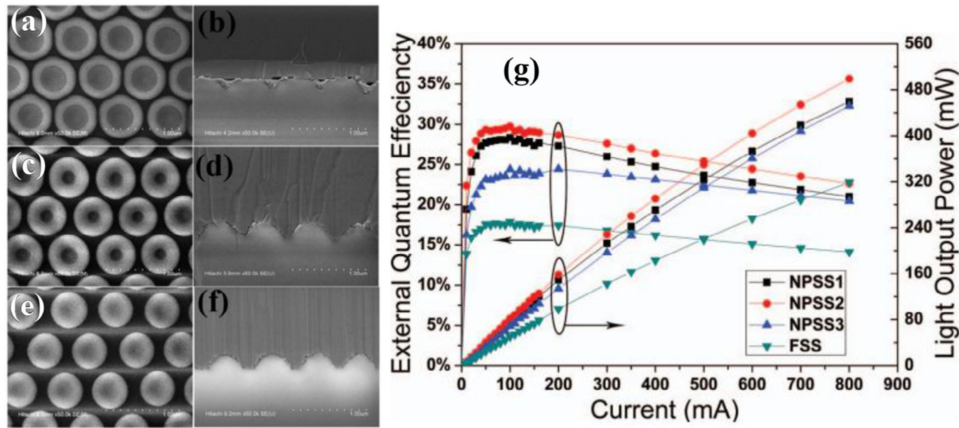


Fig. 16. Plane-view SEM images of: (a) NPSS1; (c) NPSS2; and (e) NPSS3. Cross-sectional SEM images of the GaN/NPSS interface of: (b) NPSS1; (d) NPSS2; and (f) NPSS3. (g) Light output powers and external quantum efficiencies as functions of the injection current for LEDs grown on NPSS1, NPSS2, NPSS3, and FSS (reprinted from Ref. 58 with permission of AIP).

of a large area, low cost Si substrates, non-polar GaN, and improvements of chip design are needed [60]. The GaN nanowire based LED offers advantages over its planar counterpart in the following ways. Due to the large aspect-ratio, the dislocation density within the GaN nanowire could be greatly reduced [61]. The small diameter of the nanowire also relieves the strain caused by the lattice and thermal expansion mismatch, which presents a problematic challenge when planar GaN is grown on a large area or on substrates with large differences of thermal expansion coefficient. Moreover, the active region is enclosed within the core/shell nanowire, and surface recombination is reduced. Due to the non-planar structure, LEE can be greatly improved. Furthermore, researchers have reported that multicolor LEDs can be realized on a single chip through controlling over the nanocolumn diameter from 137 to 270 nm [62].

3. Phosphor coating and fluid flow

In Section 1.3, we stated that phosphor coating is the most important fluid flow problem in LED packaging since the coating process determines the phosphor thickness, location, distribution, and morphology in LED packaging. For this coating fluid, phosphor particles are dispersed in silicone matrix, and the mixture, or phosphor gel, is a kind of non-Newton fluids. It has been validated that phosphor concentration, thickness, particle distribution and morphology influence the optical performance of LEDs greatly. Phosphor location constitutes the primary consideration in LED packaging. When altering the phosphor layer from being close to being remote to the chip, the propagation path and energy of the light will be affected in terms of the scattering and absorption of the phosphor, the reflection of the reflector, the absorption of the chip, the refraction of the lens, etc. Therefore, changing the phosphor location will affect the LEE and CCT of LEDs. Phosphor thickness and concentration are the second consideration in LEDs because the luminous flux and color of LEDs are adjusted mainly through changing the thickness and concentration. Thickness and concentration can be varied in manufacturing and will therefore affect the optical consistency of LEDs. Moreover, the dispensed phosphor gel on LED chip may have different shapes, such as planar, hemispherical, spherical cap, etc. The phosphor particles scatter the light, and thus the light propagation in different shapes of phosphor gel may be completely different. Therefore, phosphor morphology or shape also requires specific consideration.

3.1. Phosphor coating methods

Currently, there are three common methods to coat phosphor gel in LED packaging, i.e. freely dispensed coating, conformal coating and remote coating. Fig. 18 shows the schematics and pictures of the corresponding phosphor morphologies in three methods. Freely dispensed coating, as shown in Fig. 18(a), is the most convention-

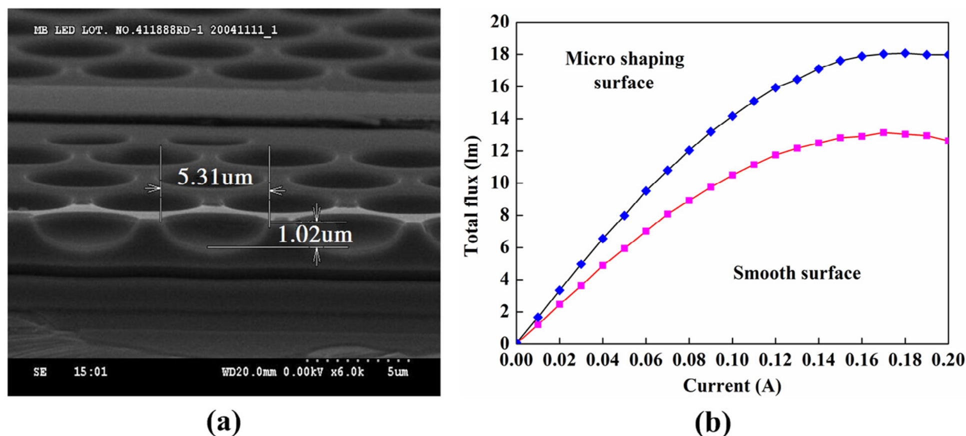


Fig. 17. SEM image of front-view of the patterned n-shaping layer. (b) Total output light flux of metal bonding type smooth surface AlGaInP LED and micro shaping surface AlGaInP LED as a function of the current in LEDs (reprinted from Ref. 59 with permission of SPIE).

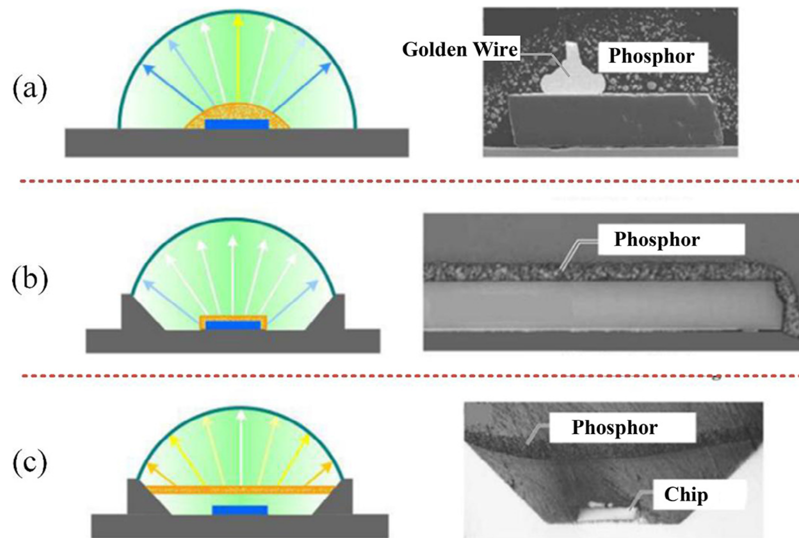


Fig. 18. Illustrations of three phosphor coating methods: (a) freely dispensed coating, (b) conformal coating, and (c) remote coating.

al method. As presented in Fig. 7, this approach dispenses phosphor silicone on the chip without a mold restricting the flow of the phosphor gel until a surface force balance is achieved. The shape of the phosphor layer is a spherical cap. Therefore, the light color from the central zone tends to be warm white, whereas the light color from the edge zone tends to be cool white. The major advantage of this method is that no special techniques are required, and thereby manufacturing time and cost are reduced. However, the primary shortcoming of this approach is also evident. Specifically, it cannot effectively control phosphor silicone volume and morphology; therefore the repeatability and consistency are relatively low and may reduce the yield of products.

Conformal coating, as shown in Fig. 18(b), is a progressive packaging process which can realize an extraordinarily thin phosphor layer. To control the final color output, the concentration of the phosphor layer is usually high due to the thin thickness. This method overcomes the nonuniform thickness of the phosphor layer in the freely dispensed method, and the angular color uniformity of the white light can be greatly enhanced. The conformal coating method was firstly developed by Lumileds, which applied the electrophoretic method [63] to deposit charged phosphor particles on the chip surface. Since controlling the voltage and deposition time can adjust the thickness of phosphor film, conformal coating can easily realize micron precision. Other developed approaches such as slurry [64], settling [65], and evaporating solvent [66] can also realize conformal phosphor coating. Although conformal coating can achieve good optical performance, it is confirmed by experiments that there is still approximately 50%–60% of light that is back-scattered by the phosphor layer [67,68]. These light rays will be re-absorbed by the chip and part of the energy is lost due to the absorption of packaging materials. Moreover, the localized heating caused by the high power chip can induce thermal quenching and reduce the quantum efficiency of the phosphor [69].

Fig. 18(c) shows the remote coating packaging. In this coating process, since only a small part of the light rays will reach the chip and be absorbed, adjusting the phosphor layer from being close to being remote to the chip can reduce the backscattering incidents and increase light extraction [70,71]. In addition, increased distance also improves color stability by lowering the surface temperature of the phosphor [72]. This coating approach normally requires a reflector to fix the phosphor layer. The main disadvantage of remote coating is that the shape of the phosphor layer is not perfectly level. Affected by the surface tension of liquid, the pre-cured encapsulant materials and phosphor layer normally present concave surfaces. Some methods can partly solve this concave surface problem such as adjusting the reflector angle, using high viscosity silicone gel, lowering the fluid temperature, etc. However, these methods cannot fundamentally solve this issue. Since the viscosity of phosphor silicone is generally higher than that of the pre-cured encapsulant, the curvature of phosphor gel will be larger, which will cause the thickness of the phosphor layer to be slightly greater in the central zones. Since the remote phosphor layer is away from the LED chips, its area is usually much larger than the area of the LED chips. Therefore, another disadvantage is that the large-area phosphor layer will disorder the light propagation and substantially deteriorate the re-emission light pattern because the well-designed optics are usually just designed for the chips or small light sources.

3.2. Fluid analysis techniques

As a viscous fluid, the flowing behavior of phosphor gel influences the phosphor coating process greatly. Elucidating this behavior will fundamentally help to realize process control. However, this flow is quite complex, as it is related to many factors, such as inertial force, capillary force, gravitational force, wettability, porosity, surface roughness, etc. To realize the flow analysis of phosphor coating, the following three techniques are necessary.

3.2.1. Fluid property analysis

Phosphor gel consists of a silicone matrix and phosphor particles, and thus its fluid property is dependent on the physical properties of silicone and phosphor parameters (concentration, particle size distribution, surface properties, etc.). In general, silicone behaves as a shear-thinning power-law fluid with a viscosity of approximately 4 Pa·s at 20 °C and surface tension of approximately 0.031 N/m. Similarly, phosphor gel also behaves as a shear-thinning power-law fluid, and its flowing process would influence the shear rate, viscosity distribution and the dynamic wetting characteristic [73,74]. However, due to silicone's thermosetting property [75] as well as the filling effect of phosphor particles, the viscosity, surface tension and rheological characteristics of phosphor gel change with the phosphor parameters and temperature.

3.2.2. Surface wettability analysis

It is well-known that surface structure substantially influences wetting properties. Fig. 19 shows a liquid droplet on a solid substrate, and there are three different phases in this case. When gravitational forces are negligible compared to surface tensions, the shape of the droplet is a spherical cap. Three surface tensions need to be considered here: solid–liquid (γ_{sl}), liquid–vapor (γ_{lv}), and solid–vapor (γ_{sv}). Young's equation [76] gives the relation between the equilibrium contact angle θ_{eq} and the three surface tensions as:

$$\gamma_{sv} = \gamma_{sl} + \gamma_{lv}\cos\theta_{eq} \tag{1}$$

When the surface tensions differ from each other; such that $\gamma_{sv}-\gamma_{sl}-\gamma_{lv} > 0$, Young's equation is not satisfied for any angle θ, and the fluid would spread over and completely wet the substrate correspondingly. For macroscopic wetting, Young's equation is sufficient to describe the wetting state of any solid–liquid–vapor system. One way of changing the surface properties and wetting state is through microtexturing. According to the wetting behaviors on the rough surfaces [77,78], two kinds of wetting states exist. When the droplets reside on the top surface of the roughness surface, this is called as Cassie–Baxter (CB) state. When the droplets impale the roughness grooves, this is called as Wenzel state. Based on the fluid properties and surface structure, we can design patterned surfaces or structured surfaces to realize the desired phosphor morphology.

3.2.3. Energy and force analysis

During the flowing process, the kinetic energy, interfacial potential energy, and gravitational potential energy are balanced by the viscous dissipation, and the energy balance equation can be written as [79]:

$$\Delta E_k(t) + \Delta E_p(t) + \Delta E_g(t) + \Delta L_f(t) = 0 \tag{2}$$

where $\Delta E_k(t)$ represents the kinetic energy variation, $\Delta E_p(t)$ is the interfacial potential energy variation, $\Delta E_g(t)$ is the gravitational potential energy variation, and $\Delta L_f(t)$ represents viscous dissipation. Among these energies, $\Delta E_g(t)$ can be neglected for tiny liquid drops; $\Delta E_k(t)$ can also be ignored for tiny liquid drops which have no impact velocity. Conservation of energy implied that, due to the viscous dissipation, the total energy of the system must decrease as the spreading process proceeds.

Regarding force analysis, the flow of droplets is controlled by capillary force, gravity, interfacial tension, viscous force and inertia force [80]. Two dimensionless numbers are often used to characterize droplet wetting dynamics – Weber number (We, $=\rho u^2 d/\gamma$) and Reynolds number (Re, $=\rho u d/\mu$). In the definitions, ρ is the density, u is the velocity, and d is the diameter of the droplet. The Weber number represents the ratio of inertia force and interfacial force, while the Reynolds number represents the ratio of inertia force and viscous force. For droplets whose diameters are larger than the capillary length (l_c, $=(\gamma/\rho g)^{1/2}$), when they are gently dropped on the surface without impact velocity, the capillary force and gravity are the main driving forces. However, when they impact on a surface, the inertia force should be taken into consideration, and the capillary effects can be neglected if $We >> Re^{1/2}$ during droplet impact [81]. For droplets whose diameters are smaller than l_c, gravity could be ignored. Capillary force and interfacial tension constitute the main driving forces in the inner flow, and the viscous force is the main resistant force during the flowing process.

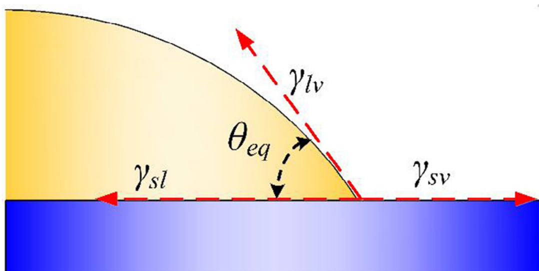


Fig. 19. Young's equation equates the surface tension forces at equilibrium.

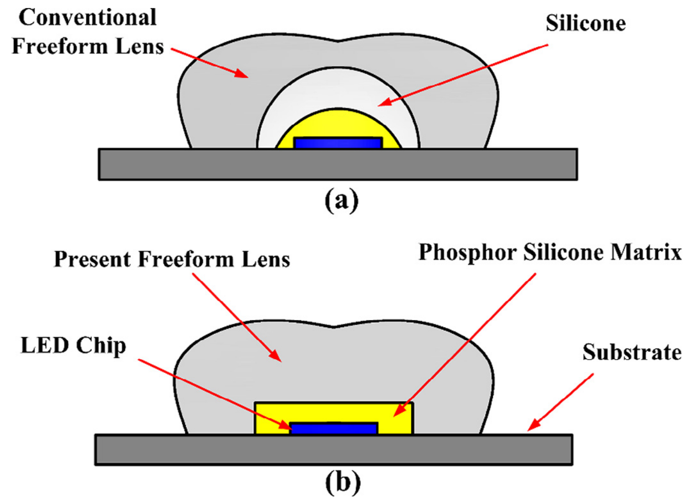


Fig. 20. (a) LED module with a conventional freeform lens where the inner surface is a hemisphere and (b) LED module with a freeform lens that can realize conformal phosphor coating.

3.3. Phosphor coating methods based on fluid analysis

To further enhance the efficiency of LED packaging, great efforts have been made to discover new processes, especially for new phosphor coating methods based on the fluid analysis.

3.3.1. Special packaging structure

Conventional phosphor coating methods usually realize a hemisphere, or spherical cap phosphor morphology, but their optical performances are limited. To overcome these limitations, some special packaging structures have been developed for realizing more optimal phosphor morphologies based on fluid properties.

Kuo et al. [82] employed a pulse spray coating method to realize a patterned remote phosphor structure, which could increase the extraction efficiency of blue rays at a large angle, and improve the stability of angular-dependent CCT. Liu et al. [83] proposed a multilayer phosphor configuration with a pyramidal shape and inverse concentration distribution. Hu et al. [84] modified the conventional Kubelka–Munk theory to analyze the phosphor layer and proposed the bi-layer structure with inverse concentration distribution to enhance the light extraction efficiency. Chen et al. [85] inserted a thin silicone layer into the dual-layer remote phosphor structure and found that this structure enhanced lumen flux by 5% at the same CCT. Wang and Huang [86] proposed a feedback coating method to stack yellow, green, and red phosphor layers, so as to realize the desired chromaticity coordinates and spectra. Hu et al. [87] realized conformal phosphor coating from the aspect of packaging lens design. Fig. 20 shows the freeform lens whose inner surface was flat rather than a conventional hemisphere, thus when filling the space between the lens and LED chip with phosphor gel, a conformal phosphor coating was formed. They used the flat inner surface to realize the conformal coating, while used the freeform outer surface to control the lighting characteristics. With accurate control of the light

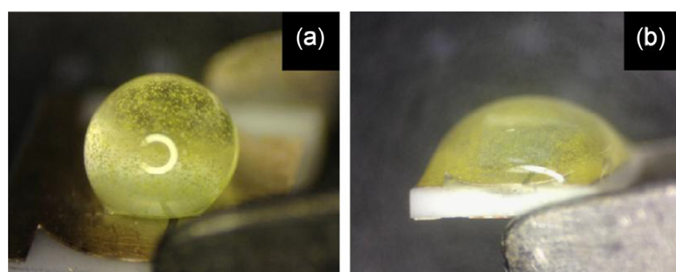


Fig. 21. Photographs of (a) spherical and (b) hemispherical phosphor silicone encapsulants (reprinted from Ref. 88 with permission of Elsevier).

path by the freeform lens, it was possible to realize phosphor conformal coating and uniform illumination simultaneously.

3.3.2. Fluid morphology control

Accurately controlling the morphology of phosphor gel constitutes an advanced approach for realizing the desired optical performance of white-light LEDs (wLEDs), since this method deals with material modification and fluid flow behaviors on a structured surface.

Huang et al. [88] added Pt nanoparticles (PtNPs) into the phosphor silicone composite and realized a spherical phosphor encapsulant for white LED packaging, and Fig. 21 shows two different phosphor morphologies with/without PtNPs. With PtNPs, as shown in Fig. 21(a), the curing reaction of the silicone was accelerated, thereby resulting in the stabilization of phosphor silicone composite quickly. While the composite without PtNP catalyst spread over the substrate, as shown in Fig. 21(b). The large surface area of the PtNPs effectively catalyzed the curing reaction of the silicone. About a 20.6% enhancement in luminous efficiency was observed. This spherical morphology was achieved based on the fluid analysis by considering the silicone's flowing and curing simultaneously. Zheng and Luo [89] proposed a new substrate structure to enhance the CCT consistency of LEDs by controlling the liquid morphology based on wetting theory. In the wetting process, the final phosphor morphology meets the rule of interfacial free energy minimization. Based on this primary rule, Zheng and Luo added two symmetrical parts on the two sides of copper slug. When the dispensed phosphor volume is too much, phosphor gel will spread along the novel structure to keep the interfacial free energy minimal, and the phosphor volume on the LED chip is consistent. Using their substrate, the variations of phosphor volume in each coating process could be greatly reduced and controlled, and thus the CCT consistency could be improved by 42.3%. Lee et al. [90] applied surface treatment to phosphors to improve the hydrophobic properties by plasmas generated from a $O\text{-}(Si(CH_3)_3)_2$ (HMDSO) plasma in a low-pressure environment. They also studied the effect of surface treatment on the total surface free energy by measuring the contact angle. It was found that plasma treatment of phosphors significantly improved the hydrophobicity of the phosphor gel (contact angle >150°) and the corresponding total surface free energy decreased substantially. Jang et al. [91] carried out hydrophobic coating on silicate-based yellow phosphors to improve the long-term stability and reliability of phosphors. After coating, the contact angle of the phosphor powder increased to 133.0° for water and 140.5° for glycerol.

3.3.3. Other typical processes for phosphor coating

3.3.3.1. Pulsed spray process. Huang et al. [92] proposed a pulsed spray (PS) process to coat a conformal phosphor on LEDs. The PS approach with an interval control is used to feed the phosphor slurry through an air atomizing nozzle to spray and pile up the phosphor layer by layer. As a result, a thin and uniform phosphor is coated along the perimeter of the chip. From their results, an accurate color distribution at a wide range of CCT (from 2500 K to 9500 K) was observed. This PS approach can also be applied to wire-bonded LED chips and an array of chips on a board (COB). The phosphor morphology coated by this PS process was shown in Fig. 22.

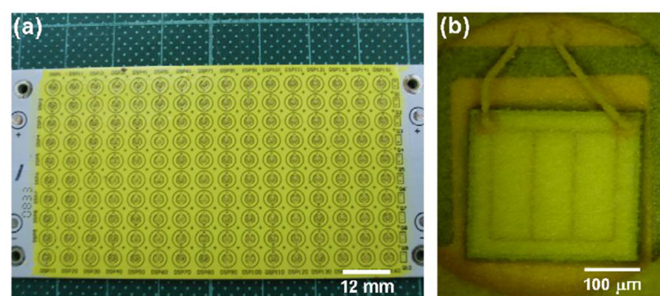
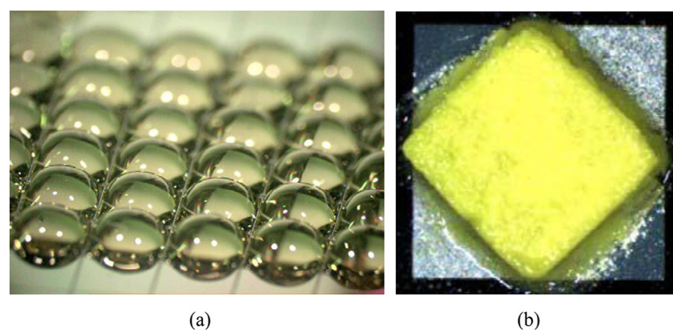


Fig. 22. Phosphor coating using the PS technique. (a) An array of blue LED chips on board (COB); and (b) the magnification of an individual LED (reprinted from Ref. 92 with permission of OSA).

3.3.3.2. Capillary microchannel process. Zheng et al. demonstrated a conformal phosphor coating method for wLEDs using a capillary microchannel [93]. The phosphor gel flowed spontaneously in the capillary microchannel and was pinned at the edge of the fixture due to the surface tension effect. With experimental validations both by conventional and vertical chips, their method could effectively improve the angular color uniformity (ACU) of the wLEDs.

3.3.3.3. Wafer-level process. In an effort to duplicate the success of integrated circuit (IC) packaging with LED packaging, the wafer-level coating process is the first attempt in terms of phosphor coating. Literally, the wafer-level process comprises coating phosphor gel on the wafer. Zhang and Lee proposed a novel encapsulation process for a wafer-level LED array [94]. The wafer substrates were fabricated by a wafer-level lithography and plating process. Their process takes advantage of square trenches fabricated by a deep reaction ion etching (DRIE) process as barriers to limit the spread of the epoxy encapsulant, and can adjust the geometry of the encapsulation via controlling the volume of the epoxy and the dimension of the trenches. The encapsulation array on a wafer is shown in Fig. 23(a). Based on the concept of screen printing, Lee and Lee developed a new methodology for coating a uniform yellow phosphor layer [95]. A silicon mold plate was fabricated with etched cavities, and served as a printing mask. The yellow phosphor powder was pushed into the apertures by a squeegee blade and bonded to the LED with UV curable epoxy. The morphology of the screen-printed phosphor layer



(a) (b)

Fig. 23. (a) Encapsulation array on a wafer (reprinted from Ref. 94 with permission of Elsevier) and (b) screen-printed phosphor layer (reprinted from Ref. 95 with permission of IEEE).

is shown in Fig. 23(b). Liu et al. developed a new structure for 3D wafer level LED packaging [96]. The structure consisted of a silicon submount wafer, a silicon cap wafer, and a layer of phosphor film. Each part was independently fabricated and subsequently assembled at the wafer-level. Experimental results indicated that the current wafer level packaging method with a remote phosphor configuration could generate white light illumination with CCT ranging from cold white to warm white. Xie et al. fabricated a novel packaging structure for wafer-level LED packaging based on Si material and a TSV array [97]. A thin layer of optical glass with phosphor was bonded to the cavity wafer. The lumen efficiency is 106 lm/W, the color rendering index is 70, and the color temperature is 4460 K. Compared to traditional LED, the advantages of this 3D integration package were good thermal diffusivity, high light efficiency, and less footprint.

In addition to the above coating methods, some other coating processes, such as electrophoresis process [63], slurry process [64], and settling process [65], have also been developed to realize some specific phosphor coating. These coating methods may have good capability in phosphor morphology control, and could realize the desired optical characteristics of LEDs. However, these methods may refer to electrical/chemical reactions rather than fluid analysis. Therefore, not much detail about these methods is provided here and interested readers may refer to Refs. 63–65.

3.4. Future trends of LED phosphor coating

Phosphor coating plays a significant role in affecting the optical/thermal performance of phosphor-converted LEDs. Obtaining a better understanding of the heat and fluid flow behaviors of phosphor gel will help to develop more highly-efficient packaging processes. Trends include: (1) application-specific coating process. Based on a full understanding and control of phosphor fluid, it may be possible to realize the optimal phosphor parameters (such as thickness, concentration, location, morphology, distribution, etc.) to achieve any desired CCT, luminous efficiency, color uniformity, etc. At the same time, the product consistency and yield will be guaranteed as well. (2) IC-compatible coating process. In the future, LEDs will be more and more widely used and the LED amounts are exponentially increasing. Analog to the success of IC packaging, LED packaging will develop more and more IC-compatible processes. Especially, the phosphor coating process will take example for some mature processes in IC packaging, such as inkjet printing, nozzle printing, offset printing, gravure printing, roll-to-roll manufacturing, etc. (3) Wafer-level coating. As mentioned above, the development of this process will simplify the packaging process, enhance product yield and reduce manufacturing cost.

4. Thermal management in LED packaging and applications

4.1. Thermal resistance network of LED lamps

There are three modes of heat transfer: conduction, convection and radiation [98]. Generally, the operating temperature of LED chips should be maintained below 120 °C, and thus heat dissipation of LED packaging through radiation could be neglected due to the relative low temperature. This implies that in LEDs, conduction and convection are the main heat transfer modes. The typical LED lamp structure is shown in Fig. 24. The LED chip is mounted onto a copper slug for heat dissipation, and is then fastened in the moulding compound as LED modules. The chip size is usually 1 mm × 1 mm, while the module is usually about 10 mm × 10 mm. Due to the high power requirement, many modules are then attached to the printed circuit board (PCB) substrate which is further bonded with a large heat sink. The sizes of the typical LED lamp change from several centimeters to meters. Thermal interface materials (TIMs) are usually chosen as the bonding materials in this architecture. Fig. 24 also shows the heat dissipation paths and thermal resistance network for LED packaging and applications. Heat generated from the chip is dissipated through two paths. Part of the heat generated in the typical leadframe LEDs will take the “upper path” to dissipate through the phosphor layer, encapsulant and optical lens; the rest of the heat is dissipated through the “lower path”, which comprises the chip, lead frame, and substrate. Since the encapsulant and phosphor layer are usually made of polymer or polymeric composites with low thermal conductivity of ~0.2 W/(m·K) [99,100], thermal resistance at the upper path is quite large. Therefore, most heat is dissipated through the “lower path”. Obviously, in the heat dissipation process, heat would conduct through many materials and interfaces.

To evaluate the system thermal resistance network, the thermal resistance network model has been developed to predict the thermal behavior of LEDs due to its low cost and high accuracy. However, this method relies on carefully considered approximations of the related heat transfer phenomena [101–108]. Christensen and Graham [109] built a thermal resistance model for Luxeon packaging LED arrays. In their work, the thermal resistance network was analyzed in order to understand the role of various thermal resistances in cooling the compact arrays. Han et al. [110] also developed a thermal resistance network model for thermal analysis of Luxeon packaging. The model was validated with the experimental data and utilized to study the effect of key parameters on the junction temperature. Using the compact thermal model, Luo et al. [111] presented an engineering approach to predict the junction temperature of high power LEDs. Detailed calculations of each thermal resistance and the total thermal resistance were validated. Regard-

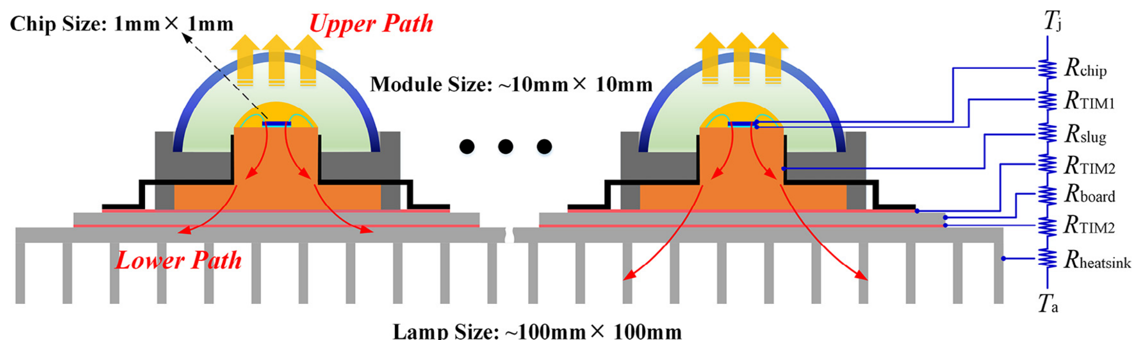


Fig. 24. Schematic of the structure and thermal resistance network of the leadframe LED based lamp.

ing the COB packaging LED arrays, Ha and Graham [112] built a thermal resistance model for thermal analysis. Using the analytical expression of thermal resistance, it is possible to determine the effect of design parameters, such as material properties, LED spacing, substrate thickness, etc., on the system thermal resistance.

In order to build the resistance network model, there are four types of resistances that should be analyzed and calculated: (1) materials bulky resistance; (2) thermal interface material (TIM) resistance; (3) thermal spreading resistance; and (4) component-to-ambient resistance. Regarding materials bulky resistance, it is usually determined by the material thermal conductivity and size. For thermal interface resistance, it is difficult to estimate due to its complicated mechanical and thermal properties. Thermal spreading resistance constitutes a key resistance in a network, which is largely dependent on the geometry of contacting bodies and the thermal boundary conditions. Fig. 24 clearly shows the large change from chip to lamp. Heat will dissipate from the small-sized chip to the large-sized lamp, and finally to the ambient. Obviously, this will lead to a large amount of thermal spreading resistance. Last, but not the least, the component-to-ambient thermal resistance predominantly reflects the heat dissipation ability of the LED lamp. The component-to-ambient resistance varies greatly from the different solutions. In this review, three typical thermal resistances are discussed specifically in the following sections, i.e., interface resistance, spreading resistance, and component-to-ambient resistance (or heat-sink resistance).

4.2. Thermal resistance of thermal interface material (TIM) and its control

4.2.1. Thermal resistance of TIM

In Fig. 24, heat generated from chips must pass through several solid–solid interfaces, such as die–slug, die–board, slug–board and board–heat sink. It is well known [113,114] that when two solid surfaces are joined, as shown in Fig. 25(a), the real contact between two bodies is established only on a few surface asperities. Consequently, the heat flux Q across such interfaces needs to be constricted at the microcontact spots. On a macroscopic scale, it brings in a temperature difference (ΔT) at the interface resulting in a thermal resistance called contact thermal resistance (R_c).

$$R_c = \Delta T/Q \tag{3}$$

To reduce R_c, a typical thermal solution is to fill the interfacial gap between the asperities with highly conductive materials, such as the thermal interface materials (TIMs). Fig. 25(b) illustrates the use of TIMs in LED packaging. The TIM 1 layer is for chip bonding, and the TIM 2 layer is utilized for the attachment of the slug to the board and the board to the heat sink. The most common TIM 1 includes solders and adhesives which require the reflow or curing process when used. Fluidic polymer-based TIMs are widely used as TIM 2, including thermal greases and phase change materials (PCMs). By inserting the TIMs into the solid surface, as shown in Fig. 25(b), a solid–TIM–solid joint forms at the surface. Fig. 25(b) shows that the TIM has a finite bond line thickness (BLT) at the joint and cannot completely fill the gap due to its inability to completely wet the surface [115]. Therefore, thermal resistance of TIM (R_{TIM}) has two components: the bulk resistance of the TIM (R_{bulk}) arising from its finite BLT and the R_c at the TIM–solid interface arising from the incomplete wetting. From Fig. 25(b), R_{TIM} can be written as:

$$R_{\mathrm{TIM}} = \frac{\mathrm{BLT}}{k_{\mathrm{TIM}}} + R_{c1} + R_{c2} \tag{4}$$

From Eq. (4), we can see that there are three factors that determine R_{TIM}: (1) R_c; (2) thermal conductivity of TIM (k_{TIM}); and (3) BLT.

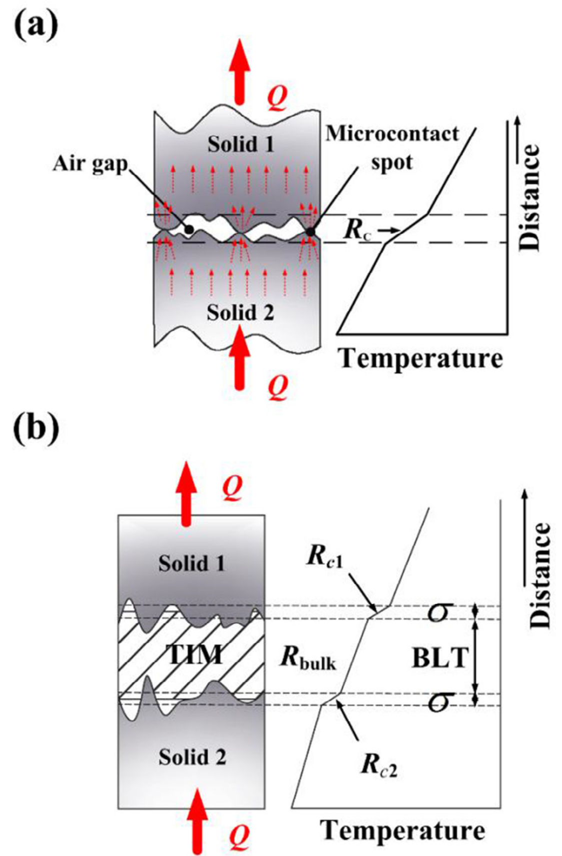


Fig. 25. Schematic showing (a) R_c at the solid–solid interface, and (b) R_{TIM} at the solid–TIM–solid joint.

One typical TIM is solder, which possesses relatively large thermal conductivity [116–118]. However, the continuing increase in packaging density of LEDs has resulted in a major challenge concerning on reliability of this interconnect material. For the solder joints, one primary factor that hinders joint reliability is the void formation during the reflow process [119–126]. Panton et al. [119] simulated void growth in molten solder bumps. The physical model in the study shows that the bubble motion is subjected to buoyancy force, drag force produced by the bulk fluid viscous flow, and the thermocapillary self-propulsion effect. The simulation results can predict the final locations and sizes of the voids after the reflow process. Experiments were also conducted to identify the locations and measure the sizes of the voids in the solder bumps [120]. It is found that the predicted results match well with the experimental findings. Ume and Jie [125] also detected the voids of solder bumps by various techniques, such as 2-D X-ray, 3-D X-ray, acoustic inspection and laser-ultrasound.

Another kind of TIM is the polymer-based TIMs which are predominantly manufactured by introducing highly thermally conductive particles such as ceramics, metals, and metal oxides into the polymer matrix [126–128]. In 2006, Prasher [129] conducted a comprehensive review of the polymer-based TIMs by discussing and analyzing the models of k_{TIM}, BLT and R_c. Since then, some progress has been made on models and new solutions for the reduction of R_{TIM}. Thus we would like to introduce the developments from the aspects of the three factors in Eq. (4) here.

4.2.1.1. R_c *models.* Past literature is replete with models of R_c at the solid–solid interface [113,114,130–133]. These studies have all asserted that R_c is a function of surface roughness, slope of asperity,

apparent area of contact, mechanical properties of solid bodies, and load between the surfaces. However, these models are not suitable for modeling the TIMs–solid contact, because the mechanical properties, such as the hardness and Young's modulus, cannot be defined for polymer-based materials which possess liquid properties.

By analyzing the models at the solid–solid contacts [113,114,131–138], the development of models should take account of both topographical and mechanical analyses at the contact. Based on the solid–solid models, some models for the liquid–solid contact have been built. Prasher [115] has modeled R_c of PCM and grease based on the definition of R_c proposed by Madhusudana [114]. Taking the wettability of the TIM on rough surface into consideration and by mechanical analysis, the model successfully illustrated the interface characteristics at the TIM–solid contact. The model is based on the surface geometry assumption that the solid asperities are conical in shape and the spacing of the peaks and valleys is equal to the roughness sampling interval. However, the roughness sampling interval cannot be used to describe surface topography because it is a profilometer parameter used to modify the roughness measurement conditions [139]. Heichal and Chandra [140] have modeled the R_c between molten metal droplets and a solid surface. In this model, the rough surface was idealized as a series of half-cylinders with same ratio placed next to each other. However, this description of surfaces was concerned that the substrates were polished with emery paper in one direction [140,141]. Recently, Hamasaiid et al. [142,143] developed a predictive model for the casting-die interface. The advantages of this model are assuming that the heights of asperity follow a Gaussian distribution which is more acceptable for describing the surface topography [113], and using a parameter, mean asperity peak spacing (R_{sm}), as the spacing of the peaks and valleys. Fig. 26(a) schematically presents the profile of the liquid–solid interface based on the topographic assumption of Hamasaiid's model [143]. Based on the definition of R_c in the CMY model [113], the authors expressed R_c as function of the effective thermal conductivity of the contacting bodies k_s, mean asperity peak spacing (R_{sm}), root-mean-square deviation of the profile (σ) and the height of entrapped air (Y) between the liquid and solid surfaces:

$$R_c = \frac{1.5\pi^2 R_{sm}\left(1-\left(\exp\left(-\frac{Y^2}{2\sigma^2}\right)-\sqrt{\frac{\pi}{2}}\frac{Y}{\sigma}\mathrm{erfc}\left(\frac{Y}{\sqrt{2}\sigma}\right)\right)\right)^{1.5}}{8k_s\mathrm{erfc}\left(\frac{Y}{\sqrt{2}\sigma}\right)\left(\exp\left(-\frac{Y^2}{2\sigma^2}\right)-\sqrt{\frac{\pi}{2}}\frac{Y}{\sigma}\mathrm{erfc}\left(\frac{Y}{\sqrt{2}\sigma}\right)\right)} \tag{5}$$

In the model, Y is found to influence R_c strongly and determined by the mechanical analysis. The analysis in Hamasaiid's model is completed by evaluating the capillarity pressure of the molten alloy as a function of the applied pressure through experiments. However, this method is difficult to apply in the estimation of Y in TIM–solid contact. Based on Hamasaiid's model, Yuan et al. [144] proposed an improved model for the prediction of R_c at the TIM–solid interface. In the model, wettability analysis at the interface was conducted to calculate Y. As shown in Fig. 26(b), when TIM impinges on the solid surface, it spreads out and wets the microcavity of the solid surface. An equilibrium state is then established at the interface among the applied pressure P, the capillarity pressure due to the surface tension of TIM γ, and the back pressure of air. By applying the ideal gas equilibrium equation on the entrapped air, it is possible to calculate the Y for the microcavities [144]. R_c at the TIM–aluminum interface was also measured for comparison with the modeling results. The modeling results were found to match the experimental data within 14.3% when the applied pressure was 0.1 MPa.

4.2.1.2. k_{TIM}. Polymer-based TIMs are filled with highly conductive particles and considered as composites. In addition to the intrinsic properties of fillers, thermal properties of composites depend on the filler loading [100,128], geometry [145,146], orientation to the thermal gradient [145,147–149], distribution [127,150–152], and interfacial properties [100,128]. Much literature exists regarding the k_{TIM} models of composites. Prasher [128] has reviewed and discussed the most common and important theoretical models, such as the Maxwell–Garnett model (MG) [153–155], Bruggeman's symmetric model (BSM) [156], Bruggeman's asymmetric model (BAM) [157], the percolation model [158–162], and the resistive network model [100,163,164]. These models focus on homogenous composites filled with randomly distributed spherical or cubic particles. However, with the increasing use of new non-spherical fillers in TIMs, such as graphene nanosheets (GNPs), boron nitride (BN) platelets and carbon nanotube (CNT), TIMs have become the heterogeneous materials with anisotropic k_{TIM}. Apart from the geometry, the anisotropic thermal property of fillers is another reason for the anisotropy of k_{TIM}. For example, GNP, with a high aspect ratio, has an in-plane thermal conductivity of ~2000 W/(m·K), whereas the through-plane thermal conductivity is less than 1 W/mK [165,166]. The experimental results [167] show that k_{TIM} of GNP-epoxy in the horizontal direction can be five times higher than that in the vertical direction when GNPs are oriented horizontally. Therefore, the geometry of fillers should be taken into consideration in developing the models.

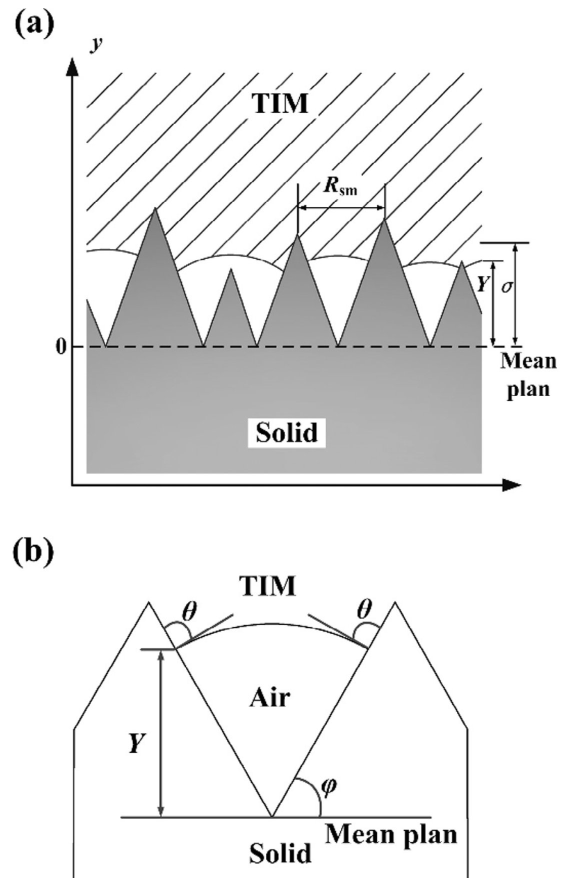


Fig. 26. Schematic of (a) profile of the TIM–solid interface; and (b) spreading of TIM on the solid rough surface.

Lewis and Nielsen (LN) [168] modified the Halpin–Tsai equation [169] to build a thermal conductivity model. Their model considers the effect of particles shape and orientation, and the type of packing for a two-phase system. However, this model does not include the interface resistance between the particle and the matrix which is found to have a dramatic effect on thermal conductivity

according to the extant literatures [100,128]. Thermal interface resistance arises from the combination of a poor mechanical or chemical adherence at the interface and a thermal expansion mismatch [100,128]. Based on the Maxwell–Garnett model [153], Nan and Birringer [170] derived an effective medium approximation (EMA) formulation for predicting the effective thermal conductivity of composites made of arbitrary ellipsoidal particles dispersed in a matrix. The formulation is for four limited cases: (1) aligned continuous fibers, (2) laminated flat plates, (3) spheres and (4) completely misoriented ellipsoidal particles. One of the advantages of the EMA formulation is that it considers the effect of interface resistance. The LN model and EMA have been applied in previous studies [171–173] for thermal conductivity prediction of composites filled with platelets or penny-shaped particles, such as BN, GNP, SiC, Al_2O_3, etc. Compared to the experimental results, the prediction of the model or formulation does not match well. According to the studies [171,173,174], a model called the Hatta–Taya (HT) model is useful in predicting the thermal conductivity of platelet-filled composites. Hatta and Taya [175] used an equivalent inclusion method to build the predictive model as expressed:

$$k^* = k_m\left(1+\frac{f}{S_i(1-f)+k_m/(k_p-k_m)}\right) \tag{6}$$

where k_m and k_p are the thermal conductivities of the matrix and particles, respectively; f is the particles volume fraction; and S_i is a factor dependent on filler shape and direction. When the matrix contains the platelet-shaped fillers, S_i can be calculated as $S_{//} = \pi p/4$ (parallel) or $S_{\perp} = 1-2S_{//}$ (perpendicular) where the variable p ($= t_p/d$) is the inverse of the particle aspect ratio, t_p and d are the thickness and diameter of the particle, respectively.

In addition to geometry and orientation, particle distribution also has a great effect on k_{TIM}. Devpura et al. [176] illustrated the effect through percolation theory [177]. As the high thermally conductive particles form a continuous chain from heat source to heat sink, there is a sudden increase in thermal conductivity. McCullough [178] also emphasized that increasing the filler concentration promotes the formation of preferential paths for heat conduction passing through the composite. Khiabani et al. [151] studied the effect of squeeze flow on the thermal properties of particulate TIMs by means of lattice Boltzmann method (LBM). They first obtained the particle distribution by simulating the squeezing process, and found that two particle stack lines form in diagonal directions. After calculating the temperature and heat flux distribution of TIMs, it is found that there was relatively lower temperature and higher heat flux in the diagonal directions.

4.2.1.3. BLT. The BLT of particle-filled TIM should depend on the rheology of the material [128]. There are four types of constitutive models used to explain the rheological behavior of polymers: (1) Newtonian fluid, (2) Power Law fluid, (3) Bingham fluid and (4) Herschel–Bulkley (H–B) fluid [179]. For these fluids with constant radii located between two substrates, the theoretical formulation of thickness has been summarized by Prasher et al. [128] It is found that Newtonian and Power Law fluid models cannot be used to model BLT of particle-filled TIM because the steady state thickness of the two fluid models is assumed as to be zero, which is unrealistic. Prasher et al. [128] found that these models underestimated the BLT of TIMs greatly and proposed a polymer rheology based empirical model:

$$\mathrm{BLT} = C\left(\frac{\tau_y}{P}\right)^M \tag{7}$$

where C and M are 1.31×10^{-4} and 0.166, respectively [130]. This model shows that BLT of particle-filled TIM depends on the yield

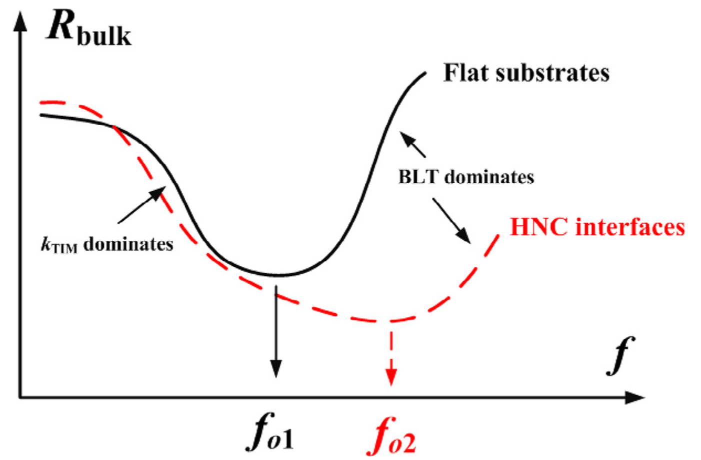


Fig. 27. Comparison of R_{bulk} of the conventional flat and hierarchical nested channel (HNC) optimized bondlines.

stress of the material τ_y and the applied pressure P. τ_y can be expressed as [179]

$$\tau_y = A\left[\frac{1}{(f_m/f)^{\frac{1}{3}}-1}\right]^2 \tag{8}$$

where A and f_m are the constant and maximum particle volume fraction, respectively. Thus τ_y depends on the particle volume fraction f. The analytical models [153–157] show that k_{TIM} of particle-filled TIM also depends on f. Many studies [128,180–183] have found that, as shown in Fig. 27, filling the TIM with a high volume fraction of particles can only be effective in decreasing R_{bulk} when the filling fraction f is less than the critical f. In this period, the filling will increase the k_{TIM} and k_{TIM} dominates the filling influence. When the filling fraction f is larger than the critical f, the BLT starts to dominate and causes R_{bulk} to increase. Therefore, when decreasing the R_{bulk}, the fillers and the fraction should be well designed.

4.2.2. Thermal resistance of TIM control

According to Eq. (4), reduction of R_{TIM} can be achieved by reducing R_c, increasing k_{TIM} and reducing BLT. Based on models [115,144], R_c can be decreased by increasing the applied pressure, using the TIMs with high surface tension and thermal conductivity, and machining the substrate with low surface roughness.

k_{TIM} is often reinforced by increasing the filler volume fraction [128]. However, as mentioned above, a high volume fraction of particles may increase the bulk resistance of TIM due to the increase of BLT. In addition to particles loading, k_{TIM} can also be reinforced by controlling the particles orientation. Inspired by the HT model [175], aligning the platelet-shaped fillers in the direction of heat load can greatly enhance the thermal performance of TIMs. As illustrated in Fig. 28, the TIM layer is expected to provide efficient heat flow from the heat source to the heat sink in the direction normal to the layer. The ideal orientation of fillers is normal to the TIM plane (Fig. 28a), whereas the isotropic and parallel orientations (Fig. 28b and 28c) are much less favorable. Several synthetic approaches have been applied to prepare the polymer composites containing the well-aligned fillers, such as electrical fields [127], magnetic fields [172], tape-casting [173], spin-coating combined with thermal imidization [174], and gravitational force [183]. Controlling the filler distribution is another effective method to increase k_{TIM}. Yung and Liem [150] enhanced the thermal conductivity of composites by filling different size particles in a matrix. Through multi-modal particle mixing, the smaller particles can fill the gaps between

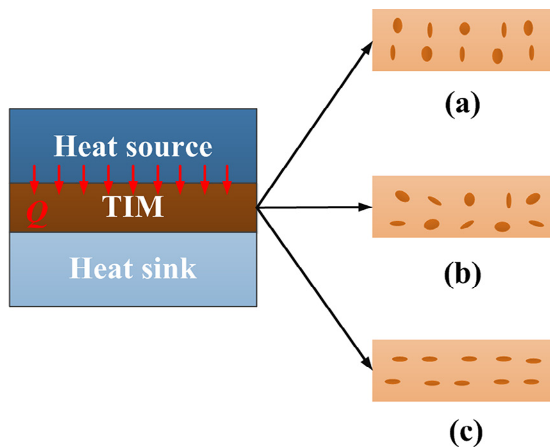


Fig. 28. Schematic of the utilization of composites sandwiched between the heat source and heat sink for heat removal. Possible orientations of platelet-shaped fillers in composites: (a) through-plane, (b) isotropic and (c) in-plane.

the bigger particles and matrix, forming the preferential paths for heat conduction. Rae et al. [152] found that thermal conductivity of the heterogeneous composites can be greater than that of composites filled with homogeneously distributed particles. The heterogeneity of composites in that work was driven by squeeze flow during which filler particles become entrapped and compacted, while the polymer matrix continues to flow. Moreover, some studies focus on the reduction of the interface resistance between matrix and fillers to increase k_{TIM}. This approach relies on the effective surface treatments for the fillers. Xu and Chung [126] made surface treatments for BN and AlN particles using acetone, acids, and silane. The results show that these treatments can increase the thermal conductivity of BN and AlN particle epoxy-matrix composites by up to 97%. Through experiments, Yung and Liem [150] also found that adding the silane coupling agent enhances the effective thermal conductivity of the polymer composite material.

Recently, a trend exists to use extremely high thermal conductivity materials, such as CNTs, tin nanowires, and graphene as the reinforcements in TIMs or TIMs directly. Biercuk et al. [184] prepared composites loaded with 1 wt% unpurified single-wall CNTs. The composites showed a 125% increase in thermal conductivity at room temperature. Feng et al. [185] produced a TIM based on double-sided array of tin nanowires. This material is prepared using a hot-pressing approach with the assistance of anodic aluminum oxide templates. The results indicate that R_{TIM} of two rough copper surfaces assisted by the tin nanowires array can reduce to 20 mm^2 K W^{-1} at 1 MPa. Shahil and Balandin [146] produced graphene–multilayer graphene nanocomposites as the highly efficient TIMs. The k_{TIM} measurements revealed a dramatic enhancement by 2300% in the graphene-based polymer at the filler loading fraction of 10 vol %.

Based on Prasher's model [128], BLT can be decreased by increasing the applied pressure and decreasing the yield stress of TIMs. However, conventional TIMs, with high particles loading, generally possess large yield stress resulting in a high BLT. Therefore, it is necessary to find effective technical solutions to reduce BLT. Through experiments, Brunschwiler et al. [186] found that two particle stack lines form in diagonal directions when the TIM is placed between two flat plates. Khiabani et al. [151] also found this phenomenon by simulations. Based on these observations, the hierarchical nested channel interface technology (HNC) [186] was proposed recently to achieve thin TIMs but with high particle loadings. In this technology, channels are machined along the bifurcation lines in one of the solid surfaces, which can prevent particle stacking and preserve material uniformity during bondline formation. By means of this technology, as seen in Fig. 27, the optimal volume fraction f_{o2} is higher than f_{o1}. In addition, Rae et al. [152] made a qualitative analysis of the particle stacking by assuming particle-filled TIM as a deformable porous media made up of the particles. They found that the squeeze rate had a great effect on the steady state BLT. In this work, the sample prepared with a relatively high squeeze rate tended to be thinner than those prepared with reduced squeeze rates.

The increase of power density and integration in LEDs requires lower total thermal resistance at the TIMs layer. A large body of research exists concerning the models and optimization of k_{TIM}. However, the increase of k_{TIM} may be not helpful for decreasing resistance. Models for R_c and BLT are still insufficient, and technical methods which focus on their reduction are scarce. Although using advanced materials as TIMs is inevitable, the exploitation of these materials should follow fundamental physical-based models to obtain their full advantages.

4.3. Thermal spreading resistance and its control

4.3.1. Thermal spreading resistance

LED chips are on the scale of millimeters, while LED modules are on the scale of centimeters, and the sizes of LED lamps may change from several centimeters to several meters. This large size difference leads to large thermal spreading resistance (R_s) in the internal heat conduction process [187]. Thermal spreading resistance, which occurs when a small heat source comes in contact with the base of a larger plate, is a key form of thermal resistance in thermal modeling of LED packages and applications. Fig. 29 shows a simulation result for such an occurrence. When the areas of the chip and the substrate are the same, the temperature is uniform throughout; however, when the chip is much smaller than the substrate, the temperature is obviously nonuniform and the hot spot phenomenon exists. R_s is an increasingly important issue in thermal management, as microelectronic/LED packages become increasingly powerful and compact. In high heat flux applications, R_s can comprise 60–70% of the total thermal resistance. When R_s is large, heat will not be distributed uniformly throughout the plate and will result in a hot spot.

4.3.2. Thermal spreading resistance control

Regarding the control of thermal spreading resistance, the first step is to develop methods to calculate or evaluate resistance. Kennedy [188] found analytical solutions in a cylinder with a constant heat flux over a part of one end and a variety of boundary conditions at the other surfaces. Kadambi and Abuaf [189] and Krane [190] obtained analytical solutions in two- and three-dimensional (2D and 3D) rectangular bodies with insulated sides and a convective boundary condition on the surface opposite to the heat input. Ellison et al. [191] derived an exact 3D solution for the steady state heat conduction equation with the source on an otherwise adiabatic surface and Newtonian cooling on the opposing surface. Muzychka et al. [192–198] studied R_s from a variety of aspects, including heat source location, boundary conditions and types of flux channel, and provided a series of analytical expressions for the calculation of R_s. These works provide methods to deal with the single LED packages and multiple LEDs or LED array.

With the formula of R_s, many methods have been developed to control thermal spreading resistance. One convenient and intuitive method is to simply increase the ratio of the heat source size to its heat sink. Based on this, it is common to use an LED array with lower single chip power to decrease R_s. Fig. 30 shows the influence of R_s on temperature distribution under different heat source distributions. It is seen in Fig. 30 that a centered heat source leads to large R_s and hotspot phenomenon, while distributed heat sources with the same power input can decrease R_s and cause a more uniform temperature distribution and a lower junction temperature. This con-

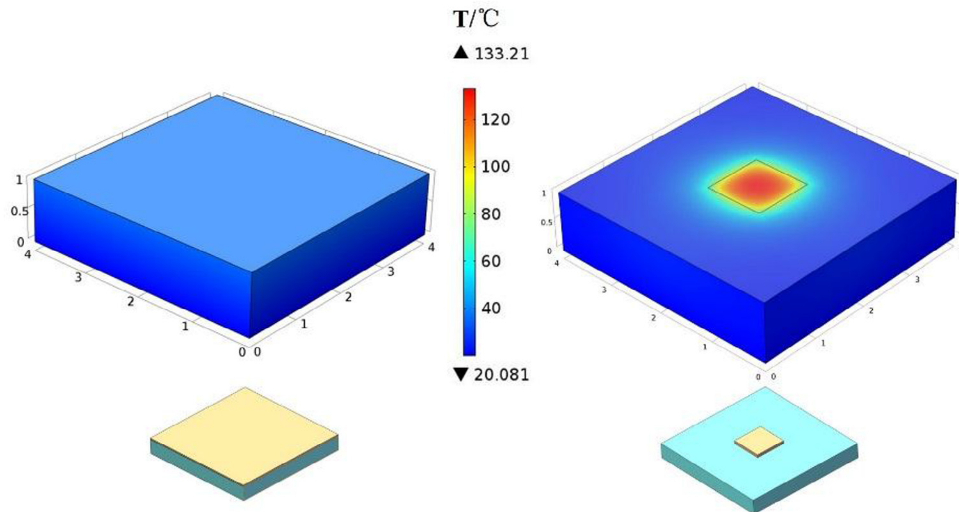


Fig. 29. Schematic diagram of R_s.

stitutes an important rule in designing LED packages and applications.

Therefore, many researchers optimized LED distribution to decrease the junction temperature according to this rule. Yang et al. [199] analyzed the effect of LED chip size on thermal spreading resistance by both simulations and experiments. They found that when the chip size increased from 15 mil to 40 mil, the total thermal resistance decreases exponentially and the thermal spreading resistance had a great effect on the total thermal resistance of LED packages. They also found that for LED modules with the same substrate thickness and power input, using graphite composite to replace aluminum as the substrate material reduced the spreading resistance by nearly 14%. Yang et al. [200] studied the thickness of copper substrate on the thermal spreading resistance in LED packages. They found that with the initial increase in copper thickness (up to 0.6 mm), the total thermal resistance (R_{cu}) of the copper substrate decreases with the copper thickness, which is attributable to the decrease in R_s. Afterwards, R_{cu} starts to lightly increase with the copper thickness, which is attributable to the increases of the bulky thermal resistance of the copper substrate. The minimum R_{cu} value occurs at the copper thickness of about 0.6 mm. Concerning LED lamps that assemble many LED modules onto a board (e.g., PCB or MCPCB), thermal spreading resistance becomes the dominant resistance since the size difference is very large. In this circumstance, it would be desirable to optimize the LED distribution to control the thermal spreading resistance. Cheng et al. [201] applied the thermal spreading resistance network to optimize the LED chip arrangement for an 80 W LED lamp. Ha and Graham [112] analyzed the thermal resistance of LED-array as a function of pitch (chip distance) by the analytical method and compared with the FEA simulations, as shown in Fig. 31. The pitch was found to be an important factor in determining the thermal resistance of LED array. Although the larger pitch can achieve a lower thermal resistance, the pitch is usually determined by considering other factors such as optical performance. For effective thermal management, it is better to minimize the interference of heat spreading in the substrate level with tuning the substrate type, thickness of each layer, etc.

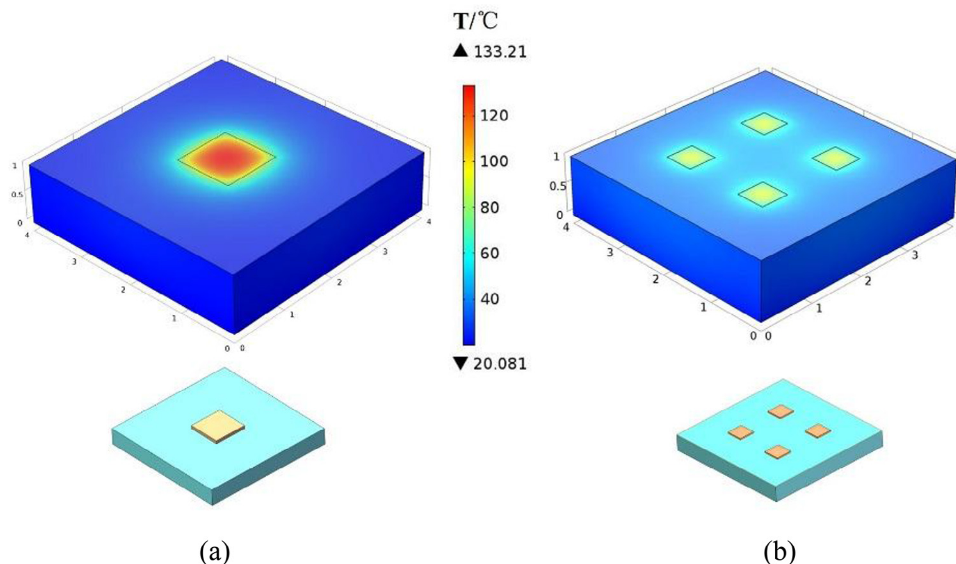


Fig. 30. Temperature distributions under different heat sources: (a) concentrated heat source; and (b) distributed heat source.

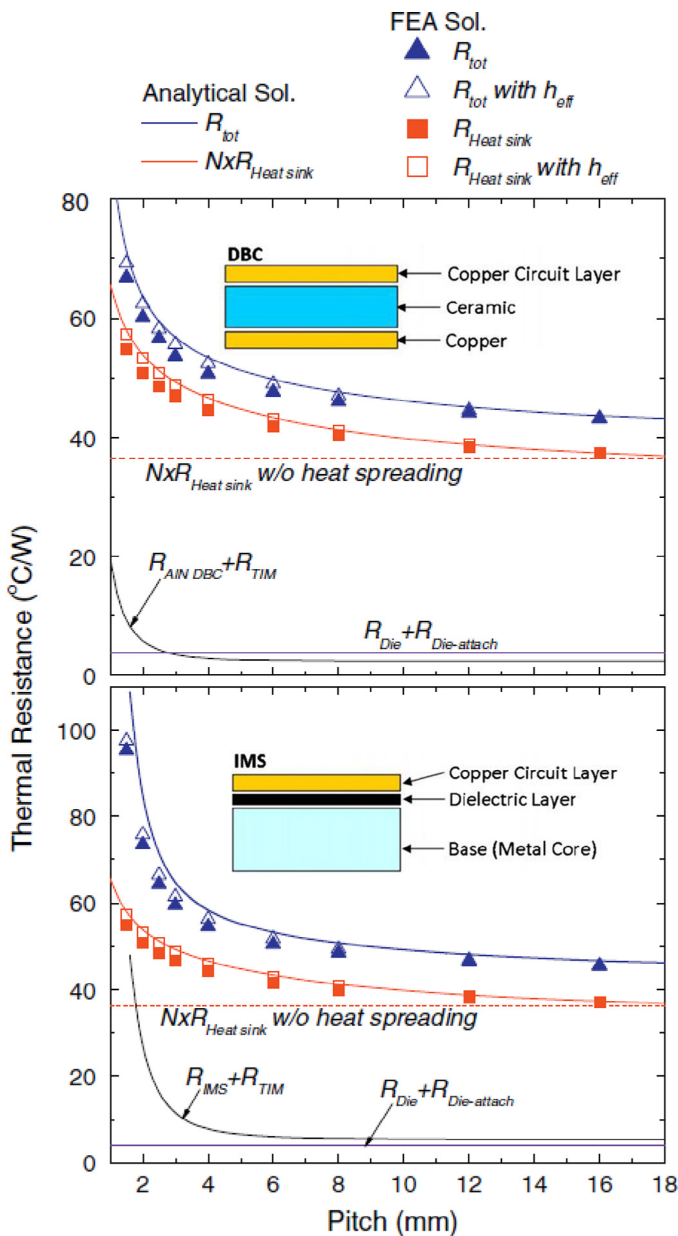


Fig. 31. Thermal resistance of LED-array as a function of pitch (chip distance) of two substrates (reprinted from Ref. 112 with permission of Elsevier).

Another method to control thermal spreading resistance comprises focusing on the substrates. However, the ability of bulky substrate optimization (e.g., material, size, structure, etc.) to control thermal spreading resistance is quite limited. The substrate coupled with some other working mechanism, such as phase change, is preferred. As a result, a flat heat pipe or vapor chamber offers an optimal solution to control thermal spreading resistance. Generally, they are fabricated as advanced substrates to assemble LEDs. A detailed discussion of these advanced solutions will be presented in the following section.

4.4. Component-to-ambient thermal resistance control

To effectively dissipate the heat in LEDs to the ambient is the ultimate goal of thermal management. The thermal resistance in this process is called component-to-ambient thermal resistance and is different from thermal solutions. In LED applications, different thermal solutions are chosen on the basis of power, heat source area, heat dissipation space, application situations, etc.

Thermal management solutions for LED applications can be divided into passive cooling and active cooling, just as the solutions for electronic devices. The key difference between these two methods is whether an external power source is needed. Passive cooling generally does not use a power source, such as a heat sink by natural convection and a heat pipe; whereas, active cooling means that there is a power source, such as forced convection with a cooling fan and liquid delivery pump. Compared to active cooling, passive cooling offers the advantages of simple structure, easy fabrication, flexibility, low cost, and high reliability. However, the heat dissipation capacity and efficiency of passive cooling are always limited by its dimensions and structure. For some high thermal density applications, passive cooling is insufficient, and active cooling is required.

4.4.1. Passive cooling

4.4.1.1. Substrate. The first component that LED chips or modules are packaged on is the substrate. Currently, LED substrates can be classified into five types [202,203]. (1) PCB (printed circuit board) is the most widely used LED substrate, which is composed of fiber glass and an epoxy resin material (FR4). FR4 is a composite material composed of woven fiberglass cloth and an epoxy resin binder, and is nearly impermeable to water. However, the thermal conductivity of FR-4 is very low (through-plane: 0.29–0.34 W/(m·K); in-plane: 0.81–1.1 W/(m·K)). The manufacturing and fabrication of PCBs are quite mature and low-cost, but its disadvantage is its poor thermal performance, resulting in low power (much less than 1 W). An inexpensive way to improve its thermal conductivity is to add thermal vias, which are created by drilling holes and copper plating them [204]. (2) MCPCBs (metal core printed circuit boards) are attached by a metal plate (Al- or Cu-thin plate) to increase thermal conductivity in PCBs. The merit of this kind of LED is that the contact surface temperature of a MCPCB is much lower than that of a PCB. However, the thermal conductivity is still at a low level because of the dielectric materials inside. (3) IMSs (insulated metal substrates) create a legal system (insulated level) by accumulating high polymer dielectric level etch copper coil electric circuits or printed circuits. This is accomplished by adhesive direct bonding on the Al- or Cu-plate with no PCB/FR4 materials in between. The thermal conductivity can be enhanced to about 1.6 W/(m·K). (4) CSs (ceramic substrates) are increasingly used as alternatives to PCB or MCPCB. In CSs, a thin layer of high polymer dielectric materials is coated onto the metal surfaces to block the electric conduction in the metal plate. The thermal conductivity of CSs could be enhanced to about 50 W/(m·K), and the CTE is about 4 ppm/K. The disadvantage of this kind of substrate is its high cost with the size limited to about 5 in^2 or below. (5) DCBS (direct copper bonded substrate) is an advanced technology. The manufacturing process passes over O_2 and N_2 to interface between the copper plate and the ceramics (Al_2O_3, AlN), and a thin layer of CuO forms with the Cu surface reaction. Then, when heated, the CuO and Al_2O_3 or AlN interact to form the insulated compound. When the dielectric level is Al_2O_3, the thermal conductivity is about 24 W/(m·K), and the CTE is about 7 ppm/K. When the dielectric level is AlN, the thermal conductivity is about 170 W/(m·K), and the CTE is about 6 ppm/K. The DCBS exhibits the best thermal performance among the above mentioned kinds of LED substrates.

4.4.1.2. Fin heat sink. Although the heat dissipation efficiency of the fin heat sink is usually limited, it is the most widely used thermal solution. In addition to passive cooling, the fin heat sink is also used in active cooling, e.g., fins are used to cool the heated working liquid in microchannels, microjets, etc. Therefore, the fin heat sink is the most fundamental method to dissipate heat to the ambient. In LED

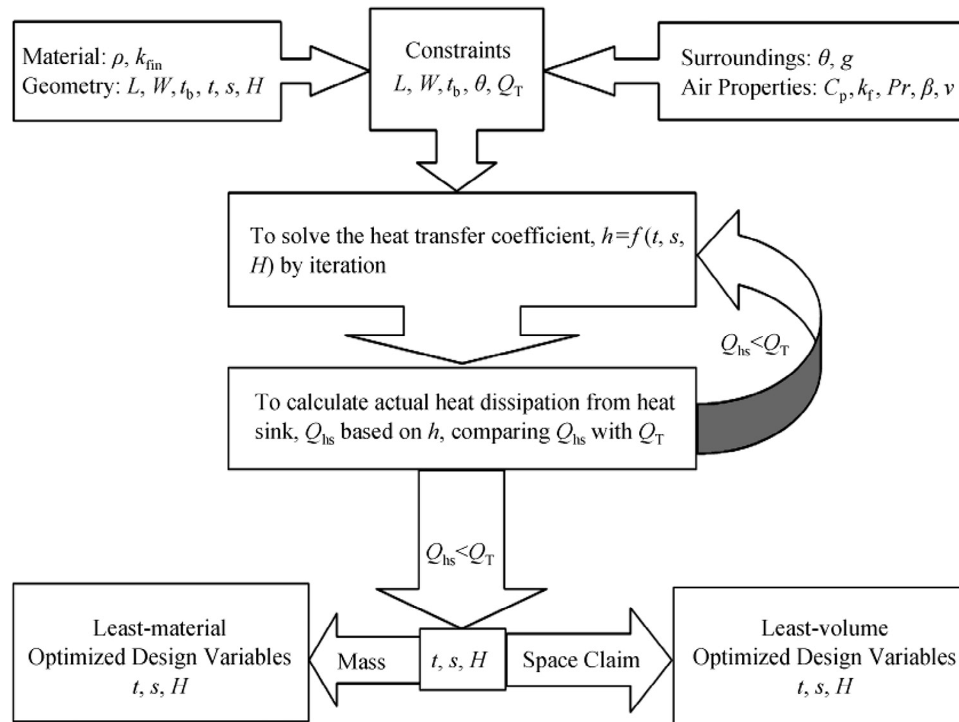


Fig. 32. Plate-fin optimization flowchart.

lamp design, placing the LED packaging onto a metallic board and then attaching it to a heat sink is recognized as a common method. Here, heat generated in LEDs is thus dissipated to the ambient from the attached heat sink via either natural convection or forced convection. So far, in LED packaging and products, studies of the fin heat sink can be classified into three categories.

4.4.1.2.1. Fin design and optimization. When selecting a proper heat sink that meets the required thermal criteria, one needs to evaluate/examine various fin parameters that affect heat sink efficiency and the overall performance of the system. Fin heat sink design methodology has been well outlined by many researchers [205–211]. Among the extensive studies on fin heat sink in LED applications, most researchers focus on the optimization of fin parameters, including spacing, height, configurations, orientation, etc., through theoretical analysis, numerical simulation, or experiments. Changing fin parameters is the most effective way to optimize fin performance, and many methods have been developed, such as the least energy method [212], the least entropy generation method [213–218], the minimum entransy dissipation-based thermal resistance principle [219–223], etc. The enhancement of fin efficiency results in the decrease of LED junction temperature directly. Charles and Wang [224] designed different fin patterns, including rectangular, trapezoidal and inverted trapezoidal configuration. They found that the heat transfer coefficient of the inverted trapezoidal fins was higher than the trapezoidal and rectangular ones by ~25% and ~10%, respectively. Luo et al. [225] developed a semi-empirical algorithm to optimize plate fin heat sink for LED street lamp application, of which the basic optimization flowchart is shown in Fig. 32. The fin height, fin thickness and fin spacing of horizontal plate fin heat sinks were designed and optimized with the aim of maximal heat dissipation and the least material. The method is based on empirical equations, and is relatively simple for engineers.

4.4.1.2.2. Fin heat sink design in specific LED applications. Considering the working characteristics of LED applications, such as chip distribution, orientation, heat flux density, and system space, some specific thermal designs were developed by simulations or experiments. Shyu et al. [226] experimentally investigated a 270 W LED backlight panel with a plate fin heat sink. Rather than the fin parameters, they analyzed the effect of shroud clearance and obstructions at the entrance or exit on overall performance were examined. This is the typical specific case for LED applications. Luo et al. [227] examined the thermal behavior of a 4 W LED bulb and then designed a heat dissipation structure for a 16 W LED bulb.

4.4.1.2.3. Special fin heat sink design with new material or structure. Some researchers improved fin efficiency by changing the working principles of the conventional fin heat sink. Yang et al. [228] brazed a layer of metal foam and carbon foam on the n fin surface. Through experiments, they found that the metal/carbon foam could enhance the heat transfer performance due to the relatively higher emissivity. Meanwhile, the weight of the heat sink was reduced as much as 33%. Yang et al. [229] developed a thermosyphon heat sink that utilized the phase change of the working liquid inside the heat sink. Their design takes advantage of the heat pipe and conventional heat sink, and thus good performance was achieved in LED street lamps. Huang et al. [230] developed a plastic fin sink which uses the enhancement of surface emissivity and geometry surface area to compensate for the deterioration of heat dissipation ability caused by the plastic materials in a 7 W LED lamp. Fig. 33 shows a fin heat sink comparison with a conventional aluminum fin heat sink. It is observed that the maximal temperature increased by 3 °C; however, the material weight and cost will be sharply decreased.

Jang et al. [231] focused on a radial heat sink for LED lighting applications, i.e., in which both convection and radiation are considered. Kim et al. [232] reports hybrid pin fins with internal channels to cool high power LEDs under natural convection or forced

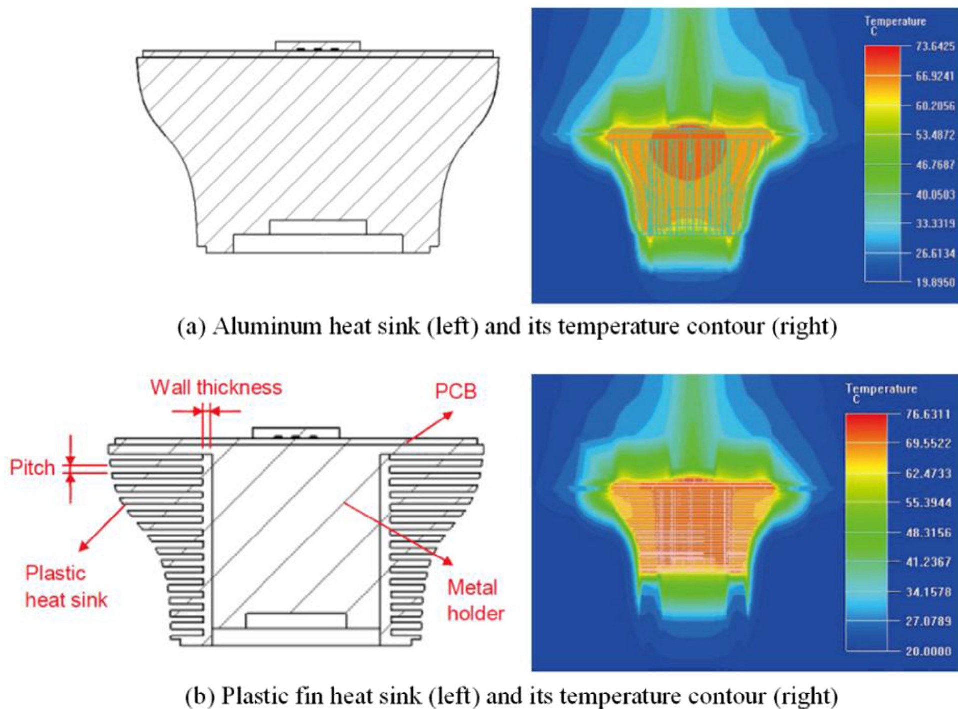


Fig. 33. Comparisons between (a) aluminum heat sink and (b) plastic fin heat sink for LED cooling (reprinted from Ref. 230 with permission of IEEE).

convection. Near the bottom of the heat sink, they drilled some holes to inhale the air. The heated air flows upward and the chimney effect was utilized to enhance heat dissipation efficiency greatly. Fig. 34 displayed this fin design. Although it is clear that the heat transfer coefficient will increase greatly due to the chimney effect, it may also raise the manufacturing costs.

4.4.1.3. Heat pipe and vapor chamber. Heat pipe technology is an advanced alternative efficient cooling method, which can transfer heat while keeping a relatively uniform temperature distribution owing to the inherent phase change heat transfer mechanism. The general working principle is that the working liquid absorbs heat in the evaporation region and changes to vapor. The vapor will flow in the whole space inside the heat pipe, and then condense to a liquid in the condensation region. The condensed liquid will then flow back to the evaporation region through wicks. Continuing this cycle, the heat in electronic devices (e.g., LEDs) will be transferred efficiently to the ambient. From the working principle, there are no moving parts in a heat pipe and simple fluids, such as water, can be used as the working fluid. There are different types of heat pipe cooling methods, such as heat pipes, loop heat pipes, vapor chambers (or called as flat plate heat pipes), but they all share the similar working principles. The difference between heat pipes and vapor chambers is that the heat transfer in heat pipes is in one dimension, but in a vapor chamber, it is in two dimensions, thus the heat transfer efficiency is enhanced greatly in vapor chambers.

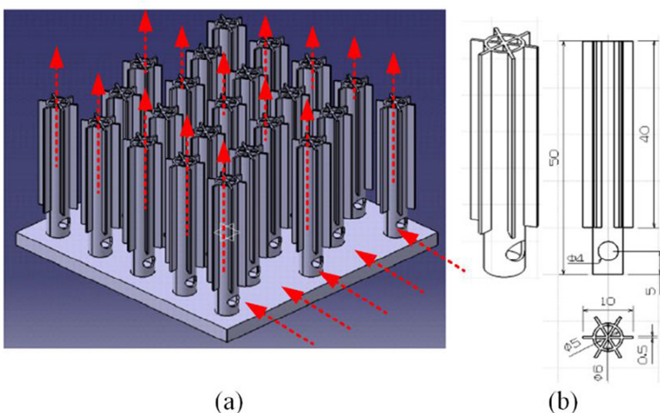


Fig. 34. Smart heat sinks (a) a 3-D view (b) structure of hybrid pin fin (reprinted from Ref. 232 with permission of IEEE).

Since heat pipes are advanced passive cooling methods that are suitable for cooling electronics, numerous studies exist on heat pipes that are applied in LED packages or products. Three categories can be identified as follows.

4.4.1.3.1. Performance study of heat pipes. For LED applications, the large difference in size between LED chips and substrate results in a large temperature difference between the LED chips and the edges of the substrates. In this situation, vapor chambers are proven to be potential alternatives to solve this problem. It is demonstrated that a sophisticated design of a vapor chamber provides an equivalent thermal conductivity of 6500–7000 W/(m·K), which is much larger than that of a metal substrate [233,234]. To fulfill this target, many researchers focused on the performance improvement of heat pipes or vapor chambers in terms of the reduction of thermal resistance. Lu et al. [235] applied a vapor chamber coupled heat sink for high power LEDs and the total thermal resistance was 8.8 K/W at 3 W. The thermal spreading resistance of a vapor chamber could be as low as 0.38 K/W from Wang and coworkers [203]. Huang et al. [236] applied a lamp-type vapor chamber to high power LED systems in natural convection, and found that thermal spreading resistance was lower than the metal plate by 34% at 30 W. Li et al. [237] fabricated a copper–water loop heat pipe (LHP) for LED illumination applications. They found that total thermal resistance ranged from 1.0 to 0.4 K/W (heating loads ranged from 30 W to 300 W). Hu et al. [238] fabricated a flat-plate vapor chamber by sintering copper powders and diffusion bonding. The transient and

steady temperature distributions of the flat plate vapor chamber were experimentally measured. The results illustrate that the vapor chamber can realize low thermal resistance (~0.3 K/W) and achieve good temperature uniformity. It could be concluded that heat pipes or vapor chambers, if well designed and fabricated, possess excellent thermal behavior in terms of heat transportation and spreading with low thermal resistance. However, in heat pipes or vapor chambers, some limitations confine thermal performance, in particular, the maximum heat transfer rate. The most obvious factors under common operations are capillary and boiling limits, as these factors will cause the dry-out phenomenon, leading to heat pipe failure. In fact, these two limitations cannot be eliminated but only postponed. By increasing the capillary pressure and permeability of the inner wick structure, the heat transfer rate may be enhanced.

4.4.1.3.2. Novel heat pipes based on new materials or structures. Yang et al. [239] investigated a polymer vapor chamber with copper micro thermal via, and found that the use of thermal via design reduced the lateral thermal resistance by 20–25%. Ye et al. [240] designed a polymer based loop heat pipe (LHP) and assembled with a silicon substrate to cool an LED package. The polymer LHP exhibited light weight and transparency, and could enhance the thermal conductivity of polymers. A group of sensors can provide accurate temperature measurement. Their present design could supply a low and relatively stable temperature to maintain higher optical power, more luminous flux and less color shift. Luo et al. [241] fabricated a silicon-glass microheat pipes (MHPs) to cool a 10 W high-power LED module. Grooves were fabricated on the silicon wafer and ionized water was chosen as the working fluid in the MHPs. Improved performance was observed with comparison experiments. Lin et al. [242] fabricated an aluminum plate oscillating heat pipes (OHPs) to cool 64 W LED modules. A series of parallel interconnected rectangular channels were manufactured as a meandering closed loop in an aluminum plate. The results showed that the LED temperature significantly decreased by natural convection when a plate OHP was used.

Liu et al. [243] studied a bionic transpiration heat pipe system for LED cooling, which is inspired by the physiological process of plant transpiration. The system consisted of the following interpretations. As shown in Fig. 35, the leaf section of a plant served as a membrane (water-permeable, micro/nano porous) across which the ambient water vapor (AWV) quasi-equilibrated with the saturated liquid water inside of the membrane under the same low pressure. A net flux of water vapor emitting into the ambient air occurred, and the pressure difference between the ambient air and the AWV was balanced by the across-membrane pressure difference and the tension of the AWV. The system enabled the extraction of water, and the extracted water evaporated on the way, absorbing a considerable amount of heat from the ambient. This comprised a heat pipe or a heat pipe cluster resembling a xylem vasculature, as indicated in Fig. 35. Their simulation results demonstrated that the bionic transpiration heat pipe used in LED cooling could maintain an average temperature below 55.6 °C.

4.4.1.3.3. Coupled with some specific LED applications. Except for the above directions, some researchers have focused on the specific application of heat pipes with LED applications. Tang et al. [244] investigated the thermal performance of LED street light modules with and without heat pipes. The improvement of heat dissipation with heat pipes was significant. Thermal resistance could be reduced by over 50% with heat pipes compared with the module without heat pipes. Fu et al. [245] designed and manufactured a 1000 W high-power LED tennis court lamp with a heat pipe-fin air cooling system. Due to the volume requirement, a large fin heat sink could be replaced by a compact one with heat pipes. Simulation results showed that the highest LED temperature was controlled at 92 °C, which could guarantee an acceptable thermal and reliability performance.

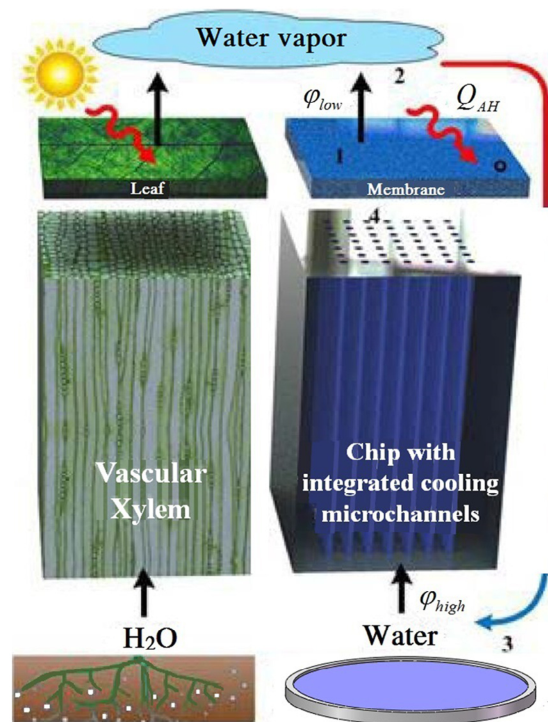


Fig. 35. Model of the bionic transpiration heat pipe (reprinted from Ref. 243 with permission of IEEE).

4.4.2. Active cooling

Not all LED applications can be passively cooled. Higher power LEDs usually require higher levels of cooling than standard heat sinks can provide. In such cases, active cooling methods are preferred due to the great enhancement in heat dissipation ability. Generally, the active cooling methods that are suitable for LEDs include forced air cooling and liquid cooling. These two methods will be discussed in detail as follows.

4.4.2.1. Forced air cooling. Forced air cooling is often necessary for applications in which the volume/surface area is small or the ambient temperature is high, and thus natural convection is inadequate to dissipate the heat in time [246–248]. Forced convection is driven by externally powered components, such as a fan or a pump, which can generate a high air flow rate and achieve one or two orders of magnitude higher heat transfer coefficient compared to that in natural convection. Therefore, forced air cooling can endure a lower temperature difference over the ambient according to Newton's cooling law. Forced air cooling systems can help provide the needed heat dissipation levels for high power LEDs, although not as quietly, dependably, or reliably as passive heat sinks cool lower power LEDs. They are not orientation-dependent, but typically cost more than passive cooling due to their complexity and power consumption. Therefore, a balance between performance and reliability needs to be considered when choosing the fin heat sink to cool LEDs light sources. In forced air cooling, a fin heat sink is usually coupled to provide a highly-efficient, highly-reliable cooling solution for LEDs. The studied on fin heat sink, whether applied in passive cooling (natural convection) or in active cooling (forced convection, forced air cooling), falls in the range of parameter optimization, new materials or structures, coupling with some specific LED application,

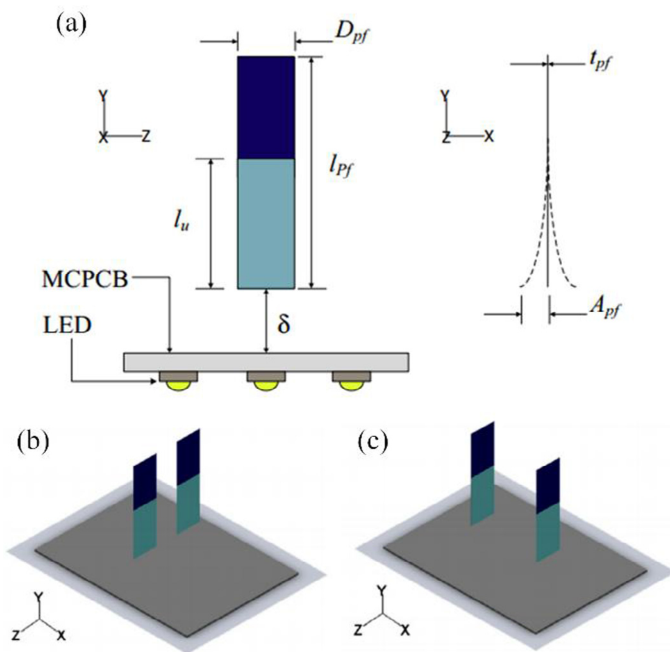


Fig. 36. (a) Schematic of the experimental setup for piezoelectric fans oriented vertically to the bottom of the LED package with different arrangements: (b) edge-to-edge and (c) face-to-face (reprinted from Ref. 250 with permission of Elsevier).

etc. Therefore, we will not describe this here, and interested readers are referred Section 4.4.1.

Instead, we would like to review studies on piezoelectric fans to generate forced air cooling. Piezoelectric fans are micro-vibrating machines used as airflow generators to help dissipate heat. They consist of a cantilever beam bonded with a piezoelectric material near their base ends. An input signal to the piezoelectric material causes oscillatory motion at the free end of the beam, and the signal could induce the surrounding flow. Acikalin et al. [249] experimentally investigated the optimal design of a single piezoelectric fan to cool LEDs. They considered different experimental configurations, fan amplitude, working distance between the fan and LED, fan length, fan frequency offset from resonance, etc. They found that applying piezoelectric fan resulted in a temperature drop at the LED of more than 36.4 °C. Sufian et al. [250] reported on the heat dissipation ability study on LED array using piezoelectric fans by both numerical and experimental methods. As shown in Fig. 36, two piezoelectric fans were vertically oriented to the LED package, i.e. edge-to-edge arrangement and face-to-face arrangement. The results showed that the single fan enhanced the average heat transfer coefficient by ~1.8 times for the LED package, and the dual fans enhanced the coefficient by ~2.3 times for edge-to-edge configuration and ~2.4 times for face-to-face configuration. Ma and Li [251] applied a dual-sided multiple fans system with a piezoelectric actuator in the thermal management of 30 W LEDs. Several parameters were discussed, including vibrating amplitude, power input, and arrangements. Ma et al. [252,253] fabricated a micro multiple piezoelectric magnetic fan (m-MPMF) to provide an innovative cooling solution to the thermal management of LED lighting. The results showed that the m-MPMF system could keep the temperature of a 9 W LEDs substrate below 55 °C, and a T-shape m-MPMF could further reduce the temperature to 45.2 °C with only 0.3 W power consumption. Wang et al. [254,255] applied the electrohydrodynamics (EHD) system to produce the ionic wind to cool LEDs. The influences of the electrode arrangement (aligned angle, distance, ground electrode configuration), electrode type, input voltage and frequency were investigated. It is found that the thermal resistance can be reduced by 50% in the LED thermal performance test.

4.4.2.2. Liquid cooling. Liquid cooling can enhance thermal management with a simple structure, transparency and small weight. Furthermore, liquid can remove the heat rather than conduct it, and thus liquid performs as better “thermal conductivity” than solid. Liquid cooling has already been successively applied in many microelectronic applications and will be easily transferred to LEDs. In some LEDs, the output power is likely to go up to 3–10 W for a single chip where the heat flux can be very high. Passive heat sinks fail to dissipate the heat in a timely manner for these LED devices except for exponentially increasing in size and weight. Under this circumstance, some liquid cooling alternatives may be appropriate. Currently, the most widely used liquid cooling methods constitute two main types, i.e. microchannel cooling and microjet cooling.

4.4.2.2.1. Microchannel cooling. Microchannel heat sinks combine the attributes of very high surface area to volume ratio, large convective heat transfer coefficient, small mass and volume, and small coolant inventory [256,257]. These attributes render these microchannels very suitable for cooling high-power LEDs or LED arrays. The microchannel heat sink cooling concept was first introduced by Tuckerman and Pease in the early 1980s [258]. Since this pioneering work, microchannel heat sinks have received considerable attention, and several studies have since been published which can be grouped as analytical [259–265], numerical [266,267], or experimental [268–277]. In applications, a microchannel heat sink often operates in the cooling system which comprises a microchannel heat sink, a micropump, a reservoir and a small heat exchanger with a fan [278,279]. In a microchannel-based heat sink, the microchannel structure plays a critical role in affecting the overall cooling capacity of the system. The most common structure is a straight fin with a rectangular cross-section. Zhang et al. [280] reported such a microchannel heat sink to cool a high-power LED array. Theoretical analysis and simulation verification were conducted and the results revealed that the minimum thermal resistance could reach 0.019 K/W. Yuan et al. [281] reported a detailed thermal analysis of LED packaging with a microchannel cooler. They also optimized the inner fin geometry inside the microchannel, flow velocity, and total power. The simulation results showed that the microchannel cooler reduced the average die temperature and the staggered fins achieved better thermal performance than the straight fins. Deng and Liu [282] proposed to use liquid metal as the coolant rather than water to cool high power LEDs. Their experimental setup was shown in Fig. 37. A series of experiments under different operational conditions were conducted to evaluate the thermal performance with comparisons to water. Under the same heat load, when using the liquid metal as the coolant, the temperature rise

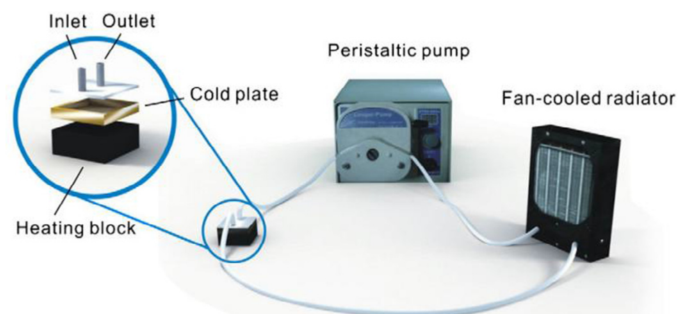


Fig. 37. Schematic of experimental setup for liquid metal cooling (reprinted from Ref. 282 with permission of Elsevier).

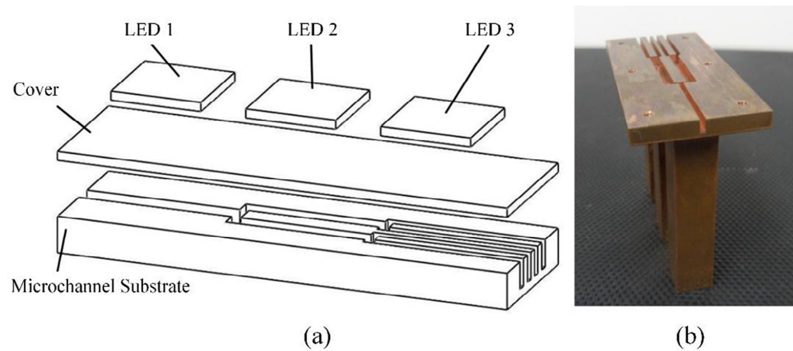


Fig. 38. Rectangular fractal tree-like microchannel substrate: (a) schematic and (b) prototype.

of LED substrates was about 13 °C, which was much lower than that based on water (about 22 °C).

In the downstream of microchannels, the temperature of the working liquid is increased and the cooling characteristics deteriorated consequently. Maintaining the uniform cooling performance of the microchannel cooling system plays an essential role in decreasing the thermal stress and enhancing consistent optical/thermal performance of multiple LEDs or LED arrays. In this situation, Luo et al. [283,284] established a compact thermal model to characterize the thermal behaviors of a rectangular fractal tree-like microchannel substrate with multiple LEDs under a target of high temperature uniformity in LEDs. The main concept is to increase the microchannel cross area to compensate for the decrease in heat transfer coefficient between the working liquid and the substrate. Thus, according to Newton's cooling law, the cooling capability may remain constant. They also fabricated prototypes and performed experiments to validate their models. The schematic and prototype of the rectangular fractal tree-like microchannel substrates are illustrated in Fig. 38.

4.4.2.2.2. Microjet cooling. The microjet cooling method offers a new method for heat flux management of the entire surface as well as hot spots of the power electronics and high-power LEDs [285,286]. Compared with the microchannel cooling system, the microjet cooling system is composed of a microjet array device, a micro-pump and a mini fluid container with a heat sink. In addition, the microjet is comparable with or better than microchannel cooling for a large target plate with a proper arrangement [287]. Luo et al. [288] performed numerical and experimental analyses of a microjet-based cooling system for the thermal management of high power LEDs. In their study, an array of 2×2 LED chips, with a size of 1×1 mm, was embedded in a 15×15 mm substrate. Their system showed a maximum increase of 36.7 °C in the chip temperature with an input power of 5.6W and a flow rate of 9.7 ml/s. Furthermore, Luo and Liu [289] carried out a parametric analysis to determine the effect of microjet diameter, top cavity height, flow rate, and the material of the device to identify an optimal design. Based on their optimal design, they fabricated the microjet cooling system to cool a 220 W LED lamp. The substrate temperature of the LED chips in the 220 W LED lamp was just 69.4 °C when the room temperature was 30.8 °C.

5. Conclusions and perspectives

In this review, the heat and fluid flow problems in LED packaging and applications were investigated. We first introduced the LED packaging processes, from which it can be seen that LED packaging comprises three aspects: (1) heat generation and dissipation; (2) fluid flowing and molding; and (3) light extraction and control; the latter one is dependent on the first two. To obtain a better understanding of the heat and fluid flow problems in LEDs, heat generation was first reviewed with some solutions to confine the heat generation. Then, the problem of phosphor gel flow was reviewed. Different phosphor coating methods and their developing trends were provided. The heat flow problem was presented in detail from three separate aspects, i.e., interface resistance, spreading resistance, and component-to-ambient resistance. The causes and corresponding solutions for these three thermal resistances were discussed.

The main objective of this review is to provide a comprehensive understanding of the heat and fluid flow problems in high-power LED packaging and applications. In fact, heat and fluid flow problems exist not only in LED packaging, but also in other electronic packaging. The attempt made here was to illustrate the basic mechanism of the heat and fluid flow characteristics, so as to assist related engineers to solve these problems fundamentally. The overall goal was divided into the following purposes: (1) to understand the mechanism of heat generation inside LED chips and to provide some ways to extract more light outside of the chips and confine the heat generation (see Section 2); (2) to summarize existing state-of-the-art phosphor coating processes and to highlight the development trends, which are based on a deep understanding of fluid flow behaviors (see Section 3); (3) to present the basic idea of controlling the heat flow problem in LED packaging (similar to IC packaging) from three aspects, i.e., controlling interface resistance, spreading resistance, and the component-to-ambient resistance (see Section 4); and (4) to develop some practical solutions to solve and control the heat flow in LEDs, so as to decrease the junction temperature and enhance reliability (see Section 4).

These conclusions do not imply that the heat and fluid flow problems in LEDs are totally understood or solved, but simply provide state-of-the-art understandings and solutions to these problems. Issues that are worth pursuing and/or exploring in the future include, but are not limited to: (1) Better LED chips. The chips could be modified for higher light extraction efficiency, and less heat generation by advanced manufacturing processes. (2) New packaging materials. New packaging materials may be developed, such as the interfacial materials, phosphors, optical components, heat spreaders, etc. (3) More efficient packaging structures. By developing some new structures, both the optical and thermal performance of LEDs may be enhanced. No matter which above issues will be broken through, it is a must to get a full understanding of heat and fluid flow problems in LEDs first since the LED packaging coupled with heat and fluid flow indeed. It is hoped that this review will help interested readers to obtain a thorough understanding of heat and fluid flow problems and to figure out where they come from and how to control them. It is only after we achieve this that we will be in the position to make our own contributions to designing

and/or manufacturing better LEDs to improve the quality of our lives.

Acknowledgement

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