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A modified bidirectional thermal resistance model for junction and phosphor temperature estimation in phosphor-converted light-emitting diodes

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ABSTRACT

Besides the junction temperature, phosphor temperature is another key parameter to characterize the thermal behavior of phosphor-converted light-emitting diodes (pc-LEDs). However, the measurement of phosphor temperature remains a challenge. In this paper, we proposed a modified bidirectional thermal resistance model for the junction and phosphor temperature estimation. Compared with the conventional thermal resistance model, both the heat generation of the phosphor layer and the heat flow through the phosphor layer were further considered in this model. Three LED packaging structures were fabricated and measured to complete the model. The heat generation of the chip and phosphor layer was measured. With varying driving current from 0.05 A to 0.65 A with an increment of 0.1 A, the maximum deviation of the predicted and measured junction and phosphor temperature is less than 1% and 9.2%, respectively, which proves the feasibility of the proposed model for the junction and phosphor temperature estimation.

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1. Introduction

Light-emitting diodes (LEDs) are widely used in general lighting and flat-panel display applications with their advantages of high luminous efficiency, long lifetime and energy saving [1–3]. In order to realize the white light illumination, a yellow phosphor layer is coated on the blue LED chip to convert the blue light to yellow light, and then the converted yellow light mixes up with the transmitted blue light, and eventually generates white light [4–7]. Such a phosphor layer coated structure is called phosphor-converted LEDs (pc-LEDs). During the color conversion process in the phosphor layer, there exists optical energy loss including the Stokes shift loss, the non-unity quantum efficiency of phosphor particles and self-absorption of yellow light by the phosphors [8]. These optical energy loss is transformed into heat, which makes the phosphor layer another heat source in the pc-LEDs. Generally, the phosphor heat generation is quite small compared to the chip heat generation. Yan et al. revealed that about 8% of the input electrical power is converted into heat by the phosphors [9]. However, such small heat in the phosphor layer can also result in extremely high local temperature due to the low thermal conductivity of the phosphor/silicone composite. High phosphor temperature will reduce the quantum conversion efficiency of the phosphors and therefore lower the luminous efficiency [10]. Moreover, it induces the material property deterioration, local stress, and even delamination, which results in the degradation of reliability and lifetime of pc-LEDs significantly [11]. Luo et al. observed that the highest temperature of the phosphor particles can reach 315.9 °C, resulting in the phosphor quenching or even the silicone carbonization [12]. Therefore, besides the junction temperature, the phosphor temperature is also an important factor to characterize the thermal performance of white pc-LEDs.

However, the phosphor temperature is difficult to measure because the phosphor particles are dispersed in the silicone matrix and the phosphor diameter usually falls in the range of 13–15 μm. The measurement of phosphor temperature has remained a challenging problem for years. There was no experimental measurement of the phosphor temperature until Kim et al. attempted to directly measure the phosphor temperature by a micro thermocouple [13]. At such circumstance, developing alternative method to predict the phosphor temperature is meaningful and urgent.

Thermal resistance model is demonstrated to be an effective tool to predict junction temperature for LED packaging [14–17]. In the conventional model [14–16], it only takes into account of the heat dissipation path from the junction layer, to the heat slug, substrate, and the ambient. Chen et al. [18] proposed a bidirectional thermal resistance model considering the bidirectional heat

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flow on both sides of the LED packaging structure and improved the accuracy of junction temperature estimation. But they did not consider the heat generation of the phosphor layer in the model. Actually, for pc-LEDs, the heat produced in the phosphor layer cannot be ignored. To solve this problem, Juntunen et al. [19] developed an improved model and considered the heat generation of phosphor layer, but here they think both the heat from the phosphor and the chip transfers from the leadframe to the ambient. Additionally, their model only focused on junction temperature estimation and did not calculate phosphor temperature.

In this work, a modified bidirectional thermal resistance model considering both the heat generation of the phosphor layer and the heat flow through the phosphor layer is proposed to estimate the junction and phosphor temperature for pc-LEDs. Experimental measurements are conducted to validate the model.

2. Model establishment

The modified model is established based on the comparison of three LED packaging structures: (I) LED chip without coating, (II) with silicone coating, and (III) with phosphor coating (i.e., pc-LED), respectively, as shown in Fig. 1. Fig. 2 illustrates the schematic of the heat flow path and the corresponding thermal resistance model of these three packaging structures.

For LED chips without any coating, one-dimensional thermal resistance model is applied, as shown in Fig. 2(I). The LED packaging structure is simplified by neglecting the internal structure and only considering a bare chip attached to a substrate with die attach adhesive (DAA). Heat generated in the chip layer is transferred from the junction layer to the ambient through conduction and convection. In this case, the total junction-to-ambience thermal resistance $R_{1,j-a}$ is introduced to define the ratio of the temperature difference between junction temperature T_j and ambient temperature T_a, to the total heat flux Q_{chip}, which can be expressed as:

$$R_{1,j-a} = \frac{T_j - T_a}{Q_{chip}} \tag{1}$$

For LED chips with silicone coating, a bidirectional thermal resistance model is applied, as shown in Fig. 2(II). There are two heat transfer paths from the junction to the ambient, namely, the lower path and the upper path. The lower path refers to the conventional pathway which is from junction through substrate to the ambient and the corresponding thermal resistance is R_{j-s-a}. And the upper path is from the junction layer through silicone coating layer to the ambient and the corresponding thermal resistance is R_{sili}. In this way, the thermal resistance of the adding silicone layer R_{sili} is connected with R_{j-s-a} in parallel. It is noted that R_{j-s-a} can be regarded as equal to $R_{1,j-a}$ for the same series of LEDs. Knowing the total junction-to-ambience thermal resistance $R_{1,j-a}$ and $R_{2,j-a}$, we can calculate R_{sili} as:

$$R_{sili} = \frac{1}{1/R_{2,j-a} - 1/R_{1,j-a}} \tag{2}$$

For LED chip with phosphor coating, a modified bidirectional thermal resistance model is proposed, as shown in Fig. 2(III). Besides the chip heat generation Q_{chip}, there is another heat source, namely the phosphor heat generation Q_{phos}. In order to express the added heat source, it is necessary to introduce the phosphor node T_{ph} which is defined as the highest temperature in the phosphor layer. We assume that all the heat dissipation of phosphor layer is generated at the phosphor node. Then Q_{phos} is divided into two parts, namely, one is from the phosphor node to the ambient Q_{ph-a} through R_{ph-a}, and the other is from the phosphor node to the junction node Q_{ph-j} through R_{ph-j}. And the heat flux component Q_{ph-j} and Q_{chip} gather into Q_{j-a}, then continues conducting downward to the ambient node. Hence, there are three heat flow branches and the heat flux of each branch satisfies the following two equations:

$$Q_{ph-a} + Q_{ph-j} = Q_{phos} \tag{3}$$

$$Q_{ph-j} + Q_{chip} = Q_{j-a} \tag{4}$$

In order to calculate T_{ph}, we should firstly determine several parameters, including T_a, Q_{chip}, Q_{phos}, R_{j-s-a}, R_{ph-j} and R_{ph-a}. The ambient temperature T_a is usually a constant which can be measured easily. Q_{chip} and Q_{phos} can be calculated by the output optical power comparison between packaging structure (II) and (III). As for the thermal resistance R_{j-s-a}, R_{ph-j} and R_{ph-a}, indirect measurements can be applied to acquire these variables. Thermal transient tester (T3ster) is used for thermal characterization of those three packaging structures, of which the total junction-to-ambience thermal resistance is $R_{1,j-a}$, $R_{2,j-a}$ and $R_{3,j-a}$, respectively. We can assume that the thermal resistance from the junction through the substrate to the ambient R_{j-s-a} of three packaging structures are all approximately equal to $R_{1,j-a}$, which can be expressed as:

$$R_{1,j-s-a} = R_{2,j-s-a} = R_{3,j-s-a} = R_{1,j-a} \tag{5}$$

For packaging structure (II) and (III), the thermal resistance of the added coating can be regarded approximately as equal, as long as two conditions are satisfied, namely, one is that both the coating share the same morphology and the other is that the phosphor volume fraction is not too high so that the thermal conductivity difference between the silicone and phosphor coating is negligible. According to Yuan's work [20,21], thermal conductivity of the phosphor/silicone composite remains stable with a slight rise when phosphor volume fraction is below 40 vol.%. In this case, the following relationships are obtained:

$$R_{ph-j} + R_{ph-a} = R_{sili} \tag{6}$$

The next step is to solve the two variables R_{ph-j} and R_{ph-a}. Based on the proposed model, junction temperature T_j can be calculated as follows:

$$T_j = T_a + R_{1,j-a} \cdot Q_{j-a} \tag{7}$$

In addition, the difference between T_j and T_a can be calculated by the product of $R_{3,j-a}$ and the total heat generation of the

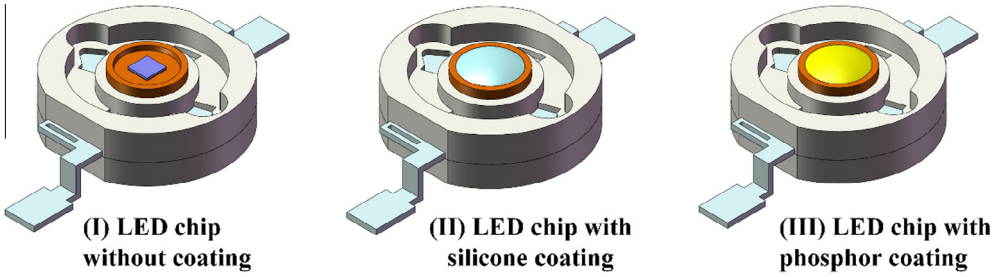

Fig. 1. Schematic of three LED packaging structures (I) LED chip without coating, (II) with silicone coating, and (III) with phosphor coating.

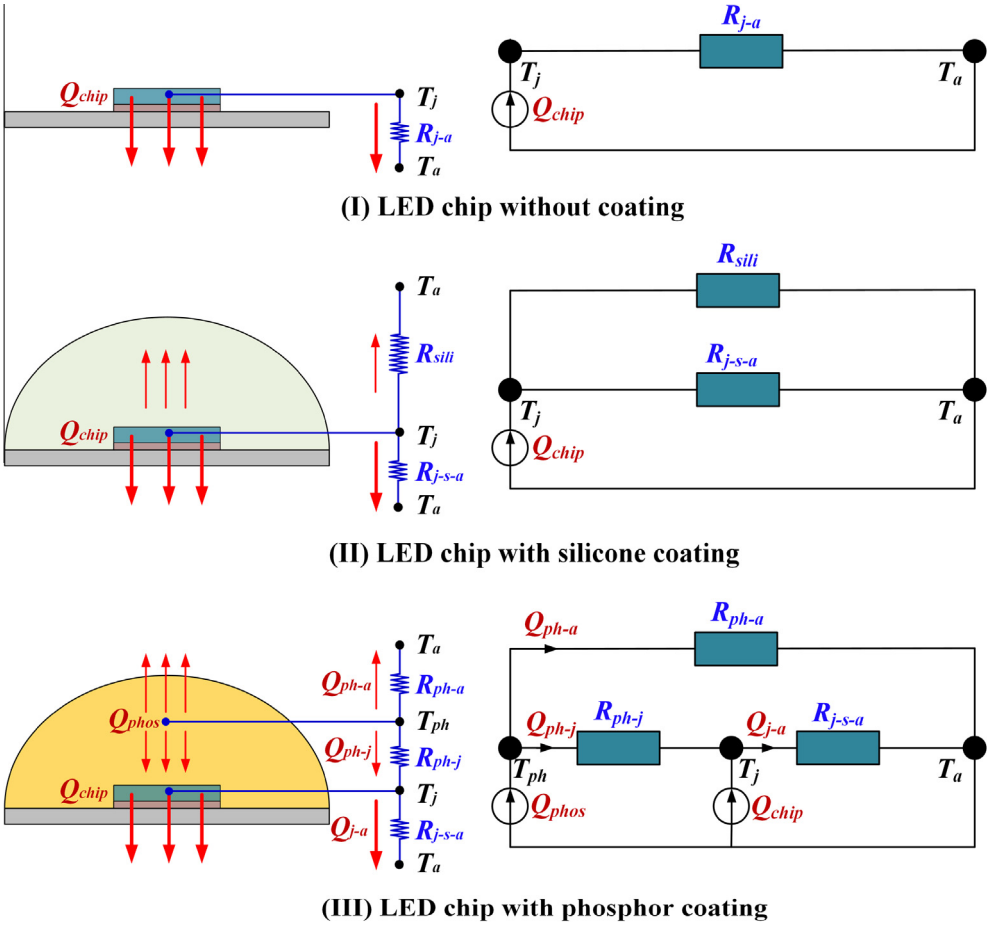

Fig. 2. Schematic of the heat flow path (left) and the corresponding thermal resistance model (right) for three LED packaging structures.

pc-LED, namely the sum of Q_{chip} and Q_{phos} [18]. Therefore, T_j can be acquired as follows:

$$T_j = T_a + R_{3,j-a} \cdot (Q_{chip} + Q_{phos}) \tag{8}$$

Combining (7) and (8), we can calculate Q_{j-a} as follows:

$$Q_{j-a} = \frac{(Q_{chip} + Q_{phos}) \cdot R_{3,j-a}}{R_{1,j-a}} \tag{9}$$

Substituting (9) to (4), we can acquire Q_{ph-j} as:

$$Q_{ph-j} = Q_{j-a} - Q_{chip} \tag{10}$$

Substituting (10) to (3), we can also acquire Q_{ph-a} as:

$$Q_{ph-a} = Q_{ph} - Q_{ph-j} \tag{11}$$

According to the model, the phosphor temperature T_{ph} can be obtained by either (12) or (13):

$$T_{ph} = T_a + Q_{ph-a} \cdot R_{ph-a} \tag{12}$$

$$T_{ph} = T_j + Q_{ph-j} \cdot R_{ph-j} \tag{13}$$

Combining (6), (8), (12), and (13), R_{ph-a} and R_{ph-j} can be calculated as:

$$R_{ph-a} = \frac{R_{3,j-a} \cdot (Q_{phos} + Q_{chip}) + R_{sili} \cdot Q_{ph-j}}{Q_{phos}} \tag{14}$$

$$R_{ph-j} = R_{sili} - R_{ph-a} \tag{15}$$

Till then, all the unknown variables are obtained and the junction and phosphor temperature for pc-LED can be calculated via (7) and (12), respectively.

3. Experimental validation

To validate the above model, three LED packaging structures were fabricated, as shown in Fig. 1. Each packaging structure possesses five samples. A volume-controlled dip-transfer coating process was applied [22] to ensure that the geometry consistency of the silicone and phosphor layer. Both the silicone and phosphor are directly coated onto the LED chip and the phosphor volume fraction is 8.5 vol.%.

To start with, the optical measurement was conducted by an integrating sphere to calculate Q_{chip} and Q_{phos}. The input electrical power P_{elec} and output optical power P_{opt} of packaging structures (II) and (III) under varying driving currents were directly measured. For those LED samples from the same batch, P_{elec} of both packaging structures under a same current is nearly equal. The output optical power of those two structures is donated as $P_{2,opt}$ and $P_{3,opt}$, respectively. Because the silicone and phosphor coating share the same geometry, the output optical power from LED chip and Q_{chip} of both structures can be regarded as equal. Moreover, when the blue light penetrates the silicone and phosphor layer, optical power loss can be defined as the difference of $P_{2,opt}$ and $P_{3,opt}$. And it is assumed that all the optical loss is occurred in the phosphor layer and converted into heat Q_{phos}, on the condition that the heat generation in substrate surface is negligible due to its high reflectance and low absorption [23]. So Q_{chip} and Q_{phos} can be calculated as follows:

$$Q_{chip} = P_{elec} - P_{2,opt} \tag{16}$$

$$Q_{phos} = P_{2,opt} - P_{3,opt} \tag{17}$$

Secondly, T3ster was used to measure the total junction-to-ambience thermal resistance of three packaging structures. Fig. 3 illustrates the experimental LED apparatus. The LED packages were attached to a designed heat sink by the thermal grease, and the heat sink had a controlled temperature of 30 °C, which was close to the ambient temperature of 29.8 °C. The thermal resistance of LED models can be obtained by evaluating the distribution of RC networks [24]. Before measurement, voltage-temperature-sensitive parameter calibration was conducted. A small current of 1 mA was applied to a temperature-controlled heat sink at different ambient temperature from 25 °C to 75 °C with an increment of 10 °C. And the measured voltage-temperature coefficient was −1.3 mV/K. The heating current for the packaging structure was from 0.05 A to 0.65 A with an interval of 0.1 A and the heating/cooling time was 20 min to ensure that the thermal stabilization was reached. In this way, the junction temperature under different driving currents can be measured.

To further verify the predicted phosphor temperature, an IR camera (FLIR SC620) was used as well. At first, the emissivity of the phosphor layer surface was calibrated and set to be 0.95. Surface temperature distribution under varying current from 0.05 A to 0.65 A with an interval of 0.1 A were obtained in the form of thermal image, in which the maximum temperature was regarded as the phosphor temperature. In this way, phosphor temperature can be measured.

4. Results and discussions

Fig. 4 shows the calculated Q_{chip} and Q_{phos} for packaging structure (III) versus driving current based on (16) and (17). It can be seen that Q_{chip} is always higher than Q_{phos}. Under the driving current of 0.65 A, Q_{chip} is about 2.5 times more than Q_{phos}, which proves that, compared with Q_{phos}, most of the heat is generated in the chip layer for pc-LEDs. Fig. 5 shows the cumulative structural function curves of three LED packaging structures under the driving current of 0.35 A. It is assumed that $R_{1,j-a}$, $R_{2,j-a}$ and $R_{3,j-a}$ are independent on the driving current. The measured results show that the average values of $R_{1,j-a}$, $R_{2,j-a}$ and $R_{3,j-a}$ are 12.37 K/W, 12.19 K/W and 11.05 K/W, respectively.

By means of the proposed model, the junction temperature and phosphor temperature can be calculated with the parameters obtained in Figs. 4 and 5. Fig. 6 illustrates the calculated and measured T_j and T_{ph} versus driving current. It can be seen that, for direct coted pc-LED, the calculated T_{ph} is always higher than the calculated T_j, which agrees with the findings of Yan's work [9]. And the rising rate of T_{ph} with current is obviously higher than that of T_j, which implies that phosphor temperature is more sensitive to current than junction temperature. It can be explained that R_{ph-a} is ten or more times than R_{j-a}, based on (7) and (12), rise of Q_{ph-a} and Q_{j-a} caused by increased current will lead to a sharper increase of T_{ph} than T_j. Under the driving current of 0.65 A, the calculated T_{ph}

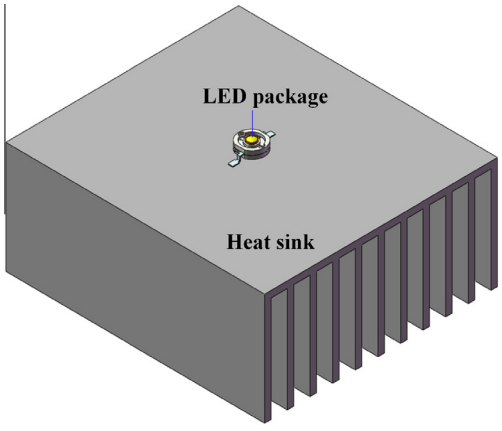

Fig. 3. Schematic of the experimental LED apparatus.

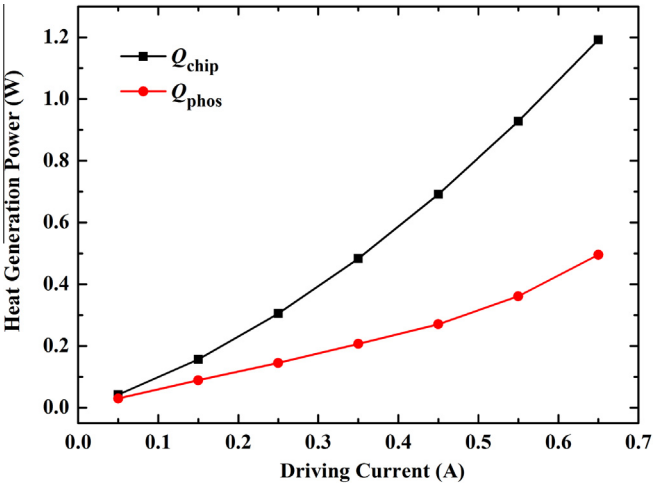

Fig. 4. The calculated Qchip and Qphos for packaging structure (III) versus driving current.

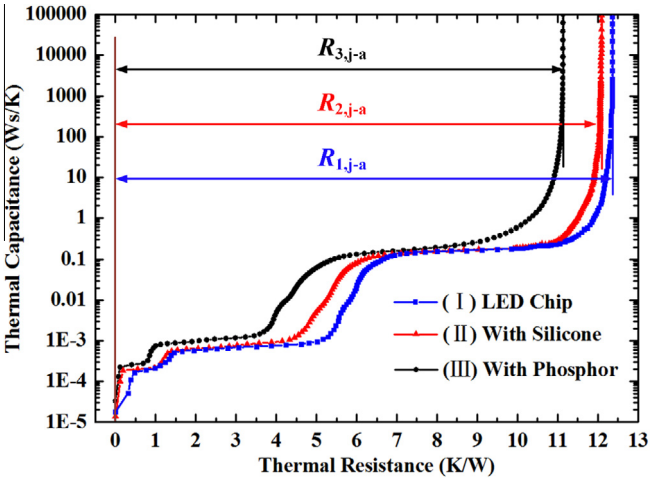

Fig. 5. The cumulative structural function curves of three LED packaging structures.

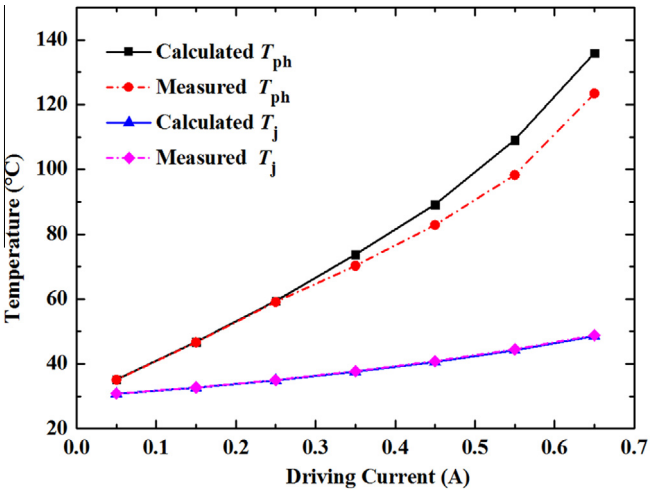

Fig. 6. The calculated and measured Tj and Tph versus driving current.

can reach 134.1 °C, which is 85.5 °C higher than the calculated T_j. When the current keeps rising, T_{ph} will exceed thermal quenching temperature of phosphors, thus leads to the failure of LED. Hence, phosphor temperature should be paid more attention in LED design and manufacturing process.

From the comparison between the calculated and measured T_j, it can be found that the maximum deviation between calculated and measured T_j was less than 1%, which means the calculation agrees pretty well with the measurement.

The measured T_{ph} obtained by the infrared thermal imager (FLIR SC620) under different currents is shown in Fig. 7. The red cursor is located at the center of the overview of LED package and its temperature is denoted as measured T_{ph}. As for the comparison between the calculated and measured T_{ph}, it can be seen that in Fig. 6, when the driving current is below 0.25 A, the temperature difference between calculation and measurement is quite small. However, as the driving current is over 0.25 A, the difference increases with rising current. And the temperature difference can reach 12.5 °C with a corresponding deviation of 9.2% when the current is 0.65 A. It can be explained that IR can only capture the surface temperature distribution of the phosphor layer, but the maximum phosphor temperature is usually located in the internal phosphor layer [9] due to the convective cooling effect on the outer surface. Therefore, the measured T_{ph} by IR is slightly lower than the calculated T_{ph}. We admit that it is better to calculate the surface temperature and to compare it with the measured phosphor temperature. But the surface temperature cannot be achieved by the present methods. It is very hard to calculate the field temperatures due to the thin phosphor layer and too many parameters coupling.

It should be noted that the temperature in this model is the maximum value, however the temperatures at different locations in the phosphor layer are different, so this model cannot precisely reflect the effect of the location on the phosphor temperature. There are some factors affecting the accuracy of the model, e.g., the heat generation Q_{chip} and Q_{phos}, and the thermal resistances $R_{1,j-a}$, $R_{2,j-a}$ and $R_{3,j-a}$.

In summary, the calculated T_j and T_{ph} agreed well with the measured T_j and T_{ph}, which proved the efficiency and accuracy of the proposed model for junction and phosphor temperature estimation. With the development of high-brightness pc-LEDs driven by high forward current, local high phosphor temperature will be a key limiting factor of the high reliability and long lifetime of LED luminaries. This modified model contributes to thermal design and packaging process improvement for reducing phosphor temperature and better thermal & optical performance of pc-LEDs.

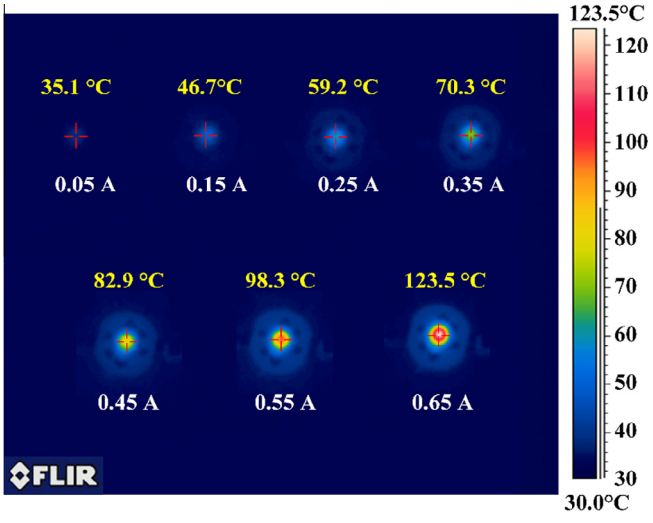

Fig. 7. Measured temperature fields of packaging structure (III) under varying driving currents.

5. Conclusion

In this work, we proposed a modified bidirectional thermal resistance model for junction and phosphor temperature prediction for pc-LEDs. The model considered the heat transfer path through the phosphor layer to the ambient and the heat generation in phosphor layer simultaneously. It covered an overall concept of heat flow and thermal resistance analysis of pc-LEDs. The junction and phosphor temperature under varying driving current from 0.05 A to 0.65 A and the constant ambient temperature of 30 °C were calculated. The modified model was validated by experiments and the calculation results agree well with the experimental results. The results show that under driving current of 0.65 A, the phosphor temperature reaches 134.1 °C, which is 85.5 °C higher than the junction temperature. We also observed that the increasing rate of phosphor temperature with rising driving current is higher than that of junction temperature, which implies that, for high-power pc-LEDs, better thermal design or packaging process is needed for lower phosphor temperature.

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